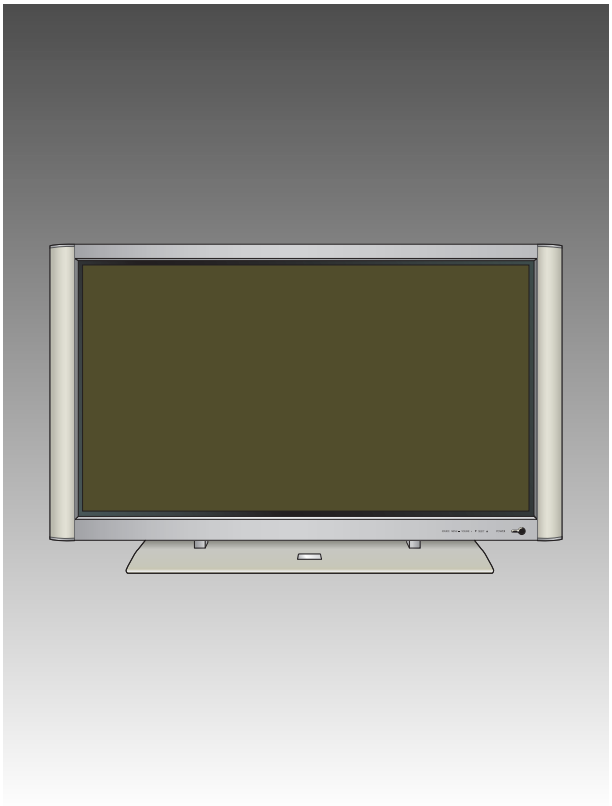
PLASMA DISPLAY TV

Chassis : **D52A**
Model: **HPL63H1X/XAA**

SERVICE Manual

PLASMA DISPLAY TV



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ELECTRONICS

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1. Precautions

Follow these safety, servicing and ESD precautions to prevent damage and protect against potential hazards such as electrical shock and X-rays.

1-1 Safety Precautions

1. Be sure that all of the built-in protective devices are replaced. Restore any missing protective shields.

2. When reinstalling the chassis and its assemblies, be sure to restore all protective devices, including: nonmetallic control knobs and compartment covers.

3. Make sure that there are no cabinet openings through which people—particularly children—might insert fingers and contact dangerous voltages. Such openings include the spacing between fornt cabinet and back cabinet, excessively wide cabinet ventilation slots, and improperly fitted back covers.

4. Leakage Current Hot Check (Figure 1-1): Warning: Do not use an isolation transformer during this test. Use a leakage-current tester or a metering system that complies with American National Standards Institute (ANSI C101.1, Leakage Current for Appliances), and Underwriters Laboratories (UL Publication UL1950.5.2).

5. With the unit completely reassembled, plug the AC line cord directly into the power outlet. With the unit's AC switch first in the ON position and then OFF, measure the current between a known earth ground (metal water pipe, conduit, etc.) and all exposed metal parts, including: antennas, handle brackets, metal cabinets, screwheads and control shafts. The current measured should not exceed 3.5 milliamp. Reverse the power-plug prongs in the AC outlet and repeat the test.

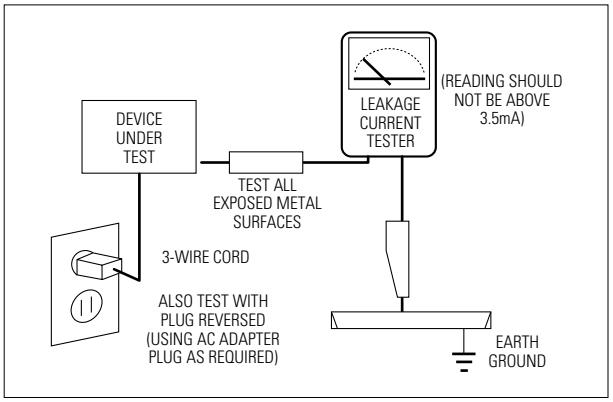


Fig. 1-1 AC Leakage Test

6. Antenna Cold Check:
With the unit's AC plug disconnected from the AC source, connect an electrical jumper across the two AC prongs. Connect one lead of the ohmmeter to an AC prong. Connect the other lead to the coaxial connector.

1-2 Safety Precautions (Continued)

7. High voltage is maintained within specified limits by close-tolerance, safety-related components and adjustments. If the high voltage exceeds the specified limits, check each of the special components.
8. Design Alteration Warning:
   Never alter or add to the mechanical or electrical design of this unit. Example: Do not add auxiliary audio or video connectors. Such alterations might create a safety hazard. Also, any design changes or additions will void the manufacturer's warranty.

9. Hot Chassis Warning:
   Some TV receiver chassis are electrically connected directly to one conductor of the AC power cord. If an isolation transformer is not used, these units may be safely serviced only if the AC power plug is inserted so that the chassis is connected to the ground side of the AC source.

   To confirm that the AC power plug is inserted correctly, do the following: Using an AC voltmeter, measure the voltage between the chassis and a known earth ground. If the reading is greater than 1.0V, remove the AC power plug, reverse its polarity and reinsert. Re-measure the voltage between the chassis and ground.

10. Some TV chassis are designed to operate with 85 volts AC between chassis and ground, regardless of the AC plug polarity. These units can be safely serviced only if an isolation transformer inserted between the receiver and the power source.

11. Some TV chassis have a secondary ground system in addition to the main chassis ground. This secondary ground system is not isolated from the AC power line. The two ground systems are electrically separated by insulating material that must not be defeated or altered.

12. Components, parts and wiring that appear to have overheated or that are otherwise damaged should be replaced with parts that meet the original specifications. Always determine the cause of damage or overheating, and correct any potential hazards.

13. Observe the original lead dress, especially near the following areas: Antenna wiring, sharp edges, and especially the AC and high voltage power supplies. Always inspect for pinched, out-of-place, or frayed wiring. Do not change the spacing between components and the printed circuit board. Check the AC power cord for damage. Make sure that leads and components do not touch thermally hot parts.

14. Product Safety Notice:
   Some electrical and mechanical parts have special safety-related characteristics which might not be obvious from visual inspection. These safety features and the protection they give might be lost if the replacement component differs from the original—even if the replacement is rated for higher voltage, wattage, etc.

   Components that are critical for safety are indicated in the circuit diagram by shading, (⚡) or (⚠).
   Use replacement components that have the same ratings, especially for flame resistance and dielectric strength specifications.
   A replacement part that does not have the same safety characteristics as the original might create shock, fire or other hazards.

15. Littum battery replace warning:
   Danger of explosion if battery is incorrectly replaced, Replace only with the same or eqivalent type.

"CAUTION, Double-pole / neutral fusing"

CAUTION

Danger of explosion if battery is incorrectly replaced.

Replace only with the same or equivalent type recommended by the manufacturer.
Dispose of used batteries according to the manufacturer's instructions.

1-3 Servicing Precautions

Warning 1 : First read the "Safety Precautions" section of this manual. If some unforeseen circumstance creates a conflict between the servicing and safety precautions, always follow the safety precautions.
Warning 2 : An electrolytic capacitor installed with the wrong polarity might explode.

1. Servicing precautions are printed on the cabinet. Follow them.

2. Always unplug the unit's AC power cord from the AC power source before attempting to: (a) Remove or reinstall any component or assembly, (b) Disconnect an electrical plug or connector, (c) Connect a test component in parallel with an electrolytic capacitor.

3. Some components are raised above the printed circuit board for safety. An insulation tube or tape is sometimes used. The internal wiring is sometimes clamped to prevent contact with thermally hot components. Reinstall all such elements to their original position.

4. After servicing, always check that the screws, components and wiring have been correctly reinstalled. Make sure that the portion around the serviced part has not been damaged.

5. Check the insulation between the blades of the AC plug and accessible conductive parts (examples: metal panels, input terminals and earphone jacks).

6. Never defeat any of the B+ voltage interlocks. Do not apply AC power to the unit (or any of its assemblies) unless all solid-state heat sinks are correctly installed.

7. Always connect a test instrument's ground lead to the instrument chassis ground before connecting the positive lead; always remove the instrument's ground lead last.

8. Plasma display panels have partial afterimages when a same picture continues to be displayed for a certain time. This happens due to the degradation of brightness caused by a scale-down effect.
   To prevent such afterimages when displaying a same picture for a certain time, be sure to reduce the level of brightness and contrast.
   ex) Contrast : 50 or 75, Brightness : 25

9. Plasma display is an array of pixels(cells). Therefore, if at least 99.9% pixels keep normal, the appropriate panel is judged as 'approved product.' Even though some of pixels keep luminescent or always light off, do not worry because the panel is approved.

1-4 Precautions for Electrostatically Sensitive Devices (ESDs)

1. Some semiconductor ("solid state") devices are easily damaged by static electricity. Such components are called Electrostatically Sensitive Devices (ESDs); examples include integrated circuits and some field-effect transistors. The following techniques will reduce the occurrence of component damage caused by static electricity.

2. Immediately before handling any semicon ductor components or assemblies, drain the electrostatic charge from your body by touching a known earth ground. Alternatively, wear a discharging wrist-strap device. (Be sure to remove it prior to applying power—this is an electric shock precaution.)

3. After removing an ESD-equipped assembly, place it on a conductive surface such as aluminum foil to prevent accumulation of electrostatic charge.

4. Do not use freon-propelled chemicals. These can generate electrical charges that damage ESDs.

5. Use only a grounded-tip soldering iron when soldering or unsoldering ESDs.

6. Use only an anti-static solder removal device. Many solder removal devices are not rated as "anti-static"; these can accumulate sufficient electrical charge to damage ESDs.

7. Do not remove a replacement ESD from its protective package until you are ready to install it. Most replacement ESDs are packaged with leads that are electrically shorted together by conductive foam, aluminum foil or other conductive materials.

8. Immediately before removing the protective material from the leads of a replacement ESD, touch the protective material to the chassis or circuit assembly into which the device will be installed.

9. Minimize body motions when handling unpackaged replacement ESDs. Motions such as brushing clothes together, or lifting a foot from a carpeted floor can generate enough static electricity to damage an ESD.

CAUTION

These servicing instructions are for use by qualified service personnel only.
To reduce the risk of electric shock do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

2. Reference Information

2-1 Tables of Abbreviations and Acronyms

Table 2-1 Abbreviations

A	Ampere	MV	Megavolt
Ah	Ampere-hour	MW	Megawatt
Å	Angstrom	MΩ	Megohm
dB	Decibel	m	Meter
dBm	Decibel Referenced to One Milliwatt	µA	Microampere
		µF	Microfarad
°C	Degree Celsius	µH	Microhenry
°F	Degree Fahrenheit	µm	Micrometer
°K	degree Kelvin	µs	Microsecond
F	Farad	µW	Microwatt
G	Gauss	mA	Milliampere
GHz	Gigahertz	mg	Milligram
g	Gram	mH	Millihenry
H	Henry	ml	Milliliter
Hz	Hertz	mm	Millimeter
h	Hour	ms	Millisecond
ips	Inches Per Second	mV	Millivolt
kWh	Kilowatt-hour	nF	Nanofarad
kg	Kilogram	Ω	Ohm
kHz	Kilohertz	pF	Picofarad
kΩ	Kilohm	lb	Pound
km	Kilometer	rpm	Revolutions Per Minute
km/h	Kilometer Per Hour	rps	Revolutions Per Second
kV	Kilovolt	s	Second (Time)
kVA	Kilovolt-ampere	V	Volt
kW	Kilowatt	VA	Volt-ampere
l	Liter	W	Watt
MHz	Megahertz	Wh	Watt-hour

Table 2-2 Table of Acronyms

ABL	Automatic Brightness Limiter
AC	Alternating Current
ACC	Automatic Chroma Control
AF	Audio Frequency
AFC	Automatic Frequency Control
AFT	Automatic Fine Tuning
AGC	Automatic Gain Control
AM	Amplitude Modulation
ANSI	American National Standards Institute
APC	Automatic Phase Control
APC	Automatic Picture Control
A/V	Audio-Video
AVC	Automatic Volume Control
BAL	Balance
BPF	Bandpass Filter
B-Y	Blue-Y
CATV	Community Antenna Television (Cable TV)
CB	Citizens Band
CCD	Charge Coupled Device
CCTV	Closed Circuit Television
Ch	Channel
CRT	Cathode Ray Tube
CW	Continuous Wave
DC	Direct Current
DVM	Digital Volt Meter
EIA	Electronics Industries Association
ESD	Electrostatic Discharge
ESD	Electrostatically Sensitive Device
FBP	Feedback Pulse
FBT	Flyback Transformer
FF	Flip-Flop
FM	Frequency Modulation
FS	Fail Safe
GND	Ground
G-Y	Green-Y
H	High
HF	High-Frequency
HI-FI	High Fidelity
IC	Inductance-Capacitance
IC	Integrated Circuit
IF	Intermediate Frequency
I/O	Input/output
L	Left
L	Low
LED	Light Emitting Diode
LF	Low Frequency
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Tr
MTS	Multi-channel Television Sound
NAB	National Association of Broadcasters
NEC	National Electric Code
NTSC	National Television Systems Committee
OSD	On Screen Display
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QIF	Quadrature Intermediate Frequency
R	Right
RC	Resistor & Capacitor
RF	Radio Frequency
R-Y	Red-Y
SAP	Second Audio Program
SAW	Surface Acoustic Wave(Filter)
SIF	Sound Intermediate Frequency
SMPS	Switching Mode Power Supply
S/N	Signal/Noise
SW	Switch
TP	Test Point
TTL	Transistor Transistor Logic
TV	Television
UHF	Ultra High Frequency
UL	Underwriters Laboratories
UV	Ultraviolet
VCD	Variable-Capacitance Diode
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VHF	Very High Frequency
VIF	Video Intermediate Frequency
VR	Variable Resistor
VTR	Video Tape Recorder
VTVM	Vacuum Tube Voltmeter
TR	Transistor

3. Specifications

3-1 Display(PDP Monitor)

MODEL		HPL6315
SCREEN SIZE		1393(H) x 783(V)/54.86 x 30.84
Dimensions (mm/inch)	Display	1566(W) x 89(D) x 912.5(H) mm/61.65(W) x 3.5(D) x 35.93(H) Inches
	Remote Control	54(W) x 31.5(D) x 220(H)mm/2.13(W) x 1.24(D) x 8.66(H) Inches
Weight	Display	72Kg/158.73lbs
	Remote Control	150g(including batteries)/0.33lbs
Power Consumption		AC120V 60Hz
Voltage		725W
RGB input		RGB1 : MINI D-SUB 15P RBG2 : BNC (R/G/B H(CS)/V) VIDEO : ANALOG 0.714V_{PP}/75 Ω(Terminated) SYNC(H,V)
VIDEO input		VIDEO : 1.0V_{PP}/75 Ω (BNC) S-VIDEO : Y -> 1.0V_{PP}/75 Ω C -> 0.28V_{PP}/75 Ω COMPONENT (Y/Pb/Pr) : Y -> 1.0V_{PP}/75 Ω Pb -> 0.7v_{PP}/75 Ω Pr -> 0.7V_{PP}/75 Ω

MEMO

5. Alignment and Adjustments

5-1 Service Mode

5-1-1 SERVICE MODE ENTRY METHOD (General Transmitter)

1. Turn off the power to make the SET STAND-BY mode.
2. In order to enter the Service Mode, select MUTE-1-8-2-POWER.

◆ In case entry into SERVICE MODE is unsuccessful, repeat the procedures above.

5-1-2 Initial DISPLAY State in times of SERVICE MODE Switch overs

INITIAL DISPLAY	PW364	SDA9280	VPC3230	SDA9400
1, PW364	Horizontal Size	CTI THRESH	BRIGHT YUV	OUT DELAY
2, SDA9280	Vertical Size	CTI TRAWID	CONT YUV	TNRCLY CLY
3, VPC3230	Horizontal Pos	Y-DELAY	IF COMP	TNRCLC CLY
4, SDA9400	Vertical Pos	LPF GAIN	Chroma Band	STOP MODE
5, CXA2101		BPF GAIN	Luma LPF	
6, AD9884		HPF GAIN	HPLL Speed	
7, OSD POSITION		PHACOM	Luma Delay	
8, OPTION		COR	3230 Bright	
9, RESET			3230 Contrast	
10, AGING			H LPF Y/C	
			H LPF Chroma	
			H Peak Filter	
			Peaking Gain	
			Coaring off/on	

CXA2101		AD9884	OSD POSITION	OPTION
Limit Level	DRIVE	RED Gain	HORIZ	1, BACK GROUND COLOR
System	SUB BRIGHT	GREEN Gain	VERT	2, SHIFT PIXEL
D - Color	SUB CONT	BLUE Gain		3, PIXEL SHIFT MIN
R - DRIVE	SUB COLOR	RED OFFSET		4, PIXEL SHIFT SEC
G - DRIVE	SUB HUE	GREEN OFFSET		5, FAN PROTECT
B - DRIVE	SUB SHP	BLUE OFFSET		6, TEMP PROTECT
R - Cut off	R - Y/R	GAIN DRIVE		7, SHARPNESS
G - Cut off	R - Y/B	OFFSET DIRVE		8, BASE LANGUAGE
B - Cut off	G - Y/R	V CONTRAST		
ABL MODE	G - Y/B	V BRIGHT		
ABL TH	PABL LEVEL	PHASE		
H SEP SEL	SHP FO	CHANGE PUMP		
CONTRAST	PRE/OVER			
BRIGHT	CTI LEVEL			
CR OFFSET1	LTI LEVEL			
CB OFFSET1	DC - TRAN			
	D - PIC			

5-1-3 Buttons Operations within SERVICE MODE

Menu	Entire menu display
Channel UP/DOWN	Cursor move to select items
Volume UP/DOWN	Enable to increase and decrease the data of the selected items

#Notice

The existing service data may be deleted after downloading a program. Be sure to make a backup copy of your data before downloading and then restore the data after completing the download.

5-1-4 White Balance Adjust Method

1. Press MUTE-1-8-2-POWER to enter the factory mode.
2. Enter AD9884
3. Adjust LOW coordinates as R, B OFFSET and HIGH coordinates as R, B GAIN.(GREEN is fixed.)
4. In AD9884, adjust brightness with V CONTRAST / V BRIGHT for VIDEO / DTV, and adjust with GAIN DRIVE / OFFSET DRIVE for PC.

- W/B Adjustment SPEC (Suwom Factory Toshiba PATTERN)

1. VIDEO MODE (SPR-3100, input TOSHIBA PATTERN)

Adjustment Coordinates	Coordinates Value	Adjustment Deviation
H-LIGHT	x : 286 y : 274 Y: 18.7(fL)	±3 ±3 ±3
L-LIGHT	x : 278 y : 272 Y: 0.53(fL)	±5 ±5 ±0.1

2. DTV MODE (SPR-3100, input TOSHIBA PATTERN)

Adjustment Coordinates	Coordinates Value	Adjustment Deviation
H-LIGHT	x : 288 y : 277 Y: 16.1(fL)	±3 ±3 ±3
L-LIGHT	x : 280 y : 277 Y: 0.71	±5 ±5 ±0.1

2. PC MODE (VG828, input TOSHIBA PATTERN)

Adjustment Coordinates	Coordinates Value	Adjustment Deviation
H-LIGHT	x : 287 y : 288 Y : 21.3(fL)	±3 ±3 ±3
L-LIGHT	x : 287 y : 294 Y : 2.17	±5 ±5 ±0.1

5-1-5 SCALAR FACTORY DATA DEFAULT VALUES

PW364

ITEM	VIDEO/S-VHS/dvd	1080I	720P	480P	PC
Horizontal Size	2	60	68	76	N/A
Vertical Size	51	48	46	52	N/A
Horizontal Pos	177	323	174	113	N/A
Vertical Pos	24	11	11	14	N/A

SDA9280

ITEM	VIDEO/S-VHS/DVD	DTV	PC
CTI THRESH	0(Fix)	-	N/A
CTI TRAWID	0(Fix)	-	N/A
Y-DELAY	10	-	N/A
LPF GAIN	7	-	N/A
BPF GAIN	8	-	N/A
HPF GAIN	10	-	N/A
PHACOM	2	-	N/A
COR	0	-	N/A

SDA9400

ITEM	VIDEO/S-VHS/DVD	DTV	PC
OUT DELAY	10	-	N/A
TNRCLY	0	-	N/A
TNRCNC	10	-	N/A
STOP MODE	3	-	N/A

VPC3230

ITEM	VIDEO/S-VHS/DVD	DTV	PC
Bright YUV	195	-	N/A
Cont YUV	29	-	N/A
IF Comp(IFC)	2	-	N/A
Chroma band(CBW)	2	-	N/A
Luma LPF(LOWP)	1	-	N/A
HPLL Speed	0	-	N/A
Luma Delay	5	-	N/A
3230 Bright	147	-	N/A
3230 Contrast	38	-	N/A
H LPF Y/C(LPF2)	0(fix)	-	N/A
H LPF Chroma(CBW2)	0	-	N/A
H Peak Filter(PFS)	(0~3) 2	-	N/A
Peaking Gain(PK)	(0~7) 3	-	N/A
Coaring Off/On	1	-	N/A

CXA2101

ITEM	VIDEO	DTV		VIDEO	DTV
Limit Level	0	-	Sub Bright (Adjustable)	(N/A)	(N/A)
System	1	2	Sub Cont	7	-
D-Color	31	-	Sub Color	2	13
R Drive	41	-	Sub Hue	7	-
G Drive	41	-	Sub SHP	2	3
B Drive	41	-	R-Y/R	7	7
R Cutoff	31	-	R-Y/B	12	12
G Cutoff	31	-	G-Y/R	7	7
B Cutoff	31	-	G-Y/B	3	3
ABL Mode	0	-	PABL Level	6	-
ABL TH	0	-	SHP FO	2	-
H sep Sel.	0	-	Pre/over	3	-
Contrast	12	-	CTI Level	1	-
Bright	52/55(480p)	-	LTI Level	0	-
Cr Offset1	3	7	DC-Tran	1	0
Cr Offset1	5	7	D-Pic	2	2
Drive (Adjustable)	(N/A)	(N/A)			

AD9884

항 목	VIDEO/S-VHS/DVD	1080i	480p	720p	PC
Red Gain	173	186	Same as left	Same as left	150
Green Gain	130 (Fixed)	130 (Fixed)	Same as left	Same as left	130 (Fixed)
Blue Gain	86	88	Same as left	Same as left	96
Red Offset	188	140	Same as left	Same as left	152
Green Offset	128 (Fixed)	128 (Fixed)	Same as left	Same as left	128 (Fixed)
Blue Offset	163	140	Same as left	Same as left	129
Gain Drive	-	-	Same as left	Same as left	200
Offset Drive	-	-	Same as left	Same as left	207
V Contrast	19	12	Same as left	Same as left	-
V Bright	38	40	Same as left	Same as left	-
Phase	15	15	15	15	-
Charge Pump	0	3(1080i) / 2(720p)	0	2	-

OSD POSITION

ITEM	VIDEO/S-VHS	DTV	PC
Horiz	40	-	-
Vert	16	-	-

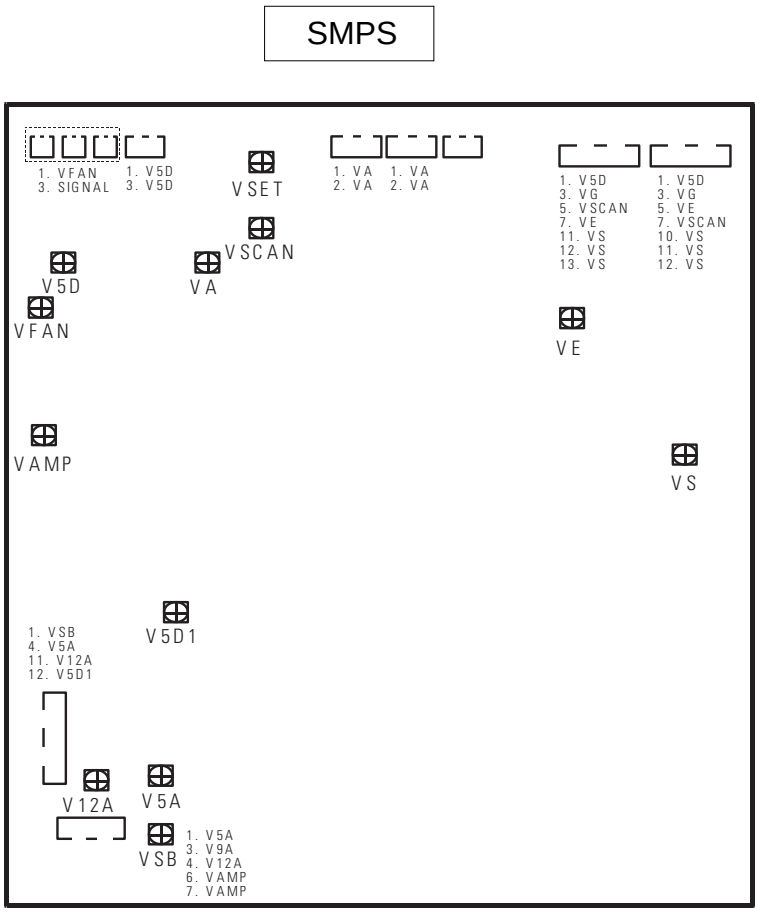
OPTION

ITEM	VIDEO/S-VHS/DVD	DTV	PC
Back Ground Color	BLUE1	-	-
Shift Pixel	4	-	-
Pixel Shift Min	4Min	-	-
Pixel Shift Min	0 Sec	-	-
Fan Protect	Off	-	-
Temp Protect	On	-	-
Sharpness	3	0	0
Base Language	English	-	-

VGA	Video signal	Dot X Line	Vertical Frequency (Hz)	Horizontal Frequency (kHz)	Vertical polarity	Horizontal polarity
1	VGA	640 X 350	70.086	31.469	N	P
2			85.080	37.861	N	P
3		640 X 400	85.080	37.861	P	N
4		720 X 400	70.087	31.469	P	N
5			85.039	37.927	P	N
6		640 X 480	59.940	31.469	N	N
7			72.809	37.861	N	N
8			75.000	37.500	N	N
9			85.008	43.269	N	N
10	WVGA	848 X 480	60.000	29.838	P	N
11			72.000	35.156	P	N
12			75.000	36.072	P	N
13			85.000	37.650	P	N
14	SVGA	800 X 600	56.250	42.925	N/P	N/P
15			60.317	37.879	P	P
16			72.188	48.077	P	P
17			75.000	46.875	P	P
18			85.061	53.674	P	P
19	XGA	1024 X 768	60.004	48.363	N	N
20			70.069	56.476	N	N
21			75.029	60.023	P	P
22			84.997	68.677	P	P
23		1152 X 864	75.000	67.500	P	P
24	WXGA	1280 X 768	60	47.700	P	N
25			75	60.150	P	N
26	SXGA	1280 X 1024	60.020	63.981	P	P
27			75.025	79.976	P	P

5-2 Adjusting the Discharge Voltage Of the Main Unit While Replacing ASS'Y (Body Part)

◆ Turning the variable resistor clockwise reduces voltage except VG, V9, and VR(6).



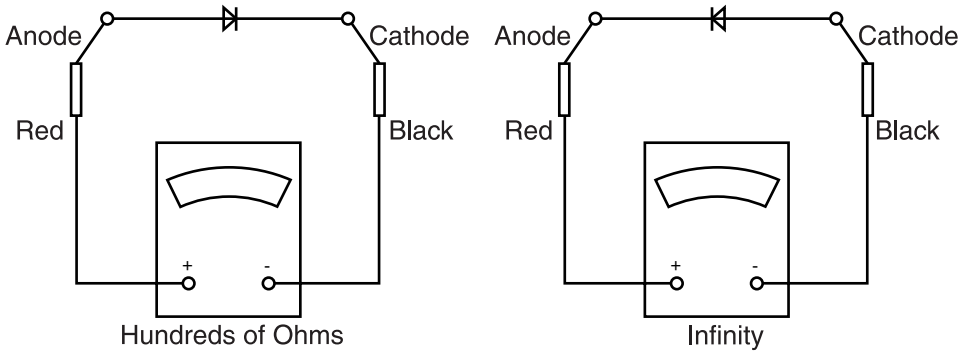
OUTPUT	Voltage(V)
VS	168
VE	183
VA	70
VSET	190
VSCAN	80
V5D	5
VFAN	12
VAMP	9
V5D1	5
V5A	5
V12A	12
VSB	5

Alignment and Adjustments

5-3 Fault Finding Using MULTI METER

Parts defects can be found for DIODE TRANSISTOR IC, using MULTI TEST including Forward / Reverse direction Multi Test. Of course, in case resistance of several ohms and COIL are connected in parallel circuit, the lock out circuit parallel connected to part must be severed.

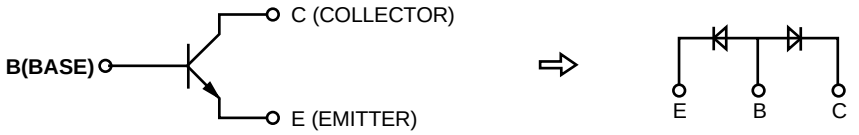
1.DIODE



	Forward Direction	Reverse Direction
Between Anode and Cathode	Hundreds of ohms	Infinity

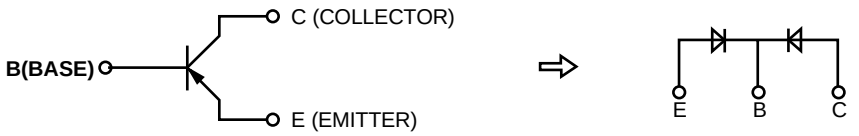
2. TRANSISTOR

● For NPN(KSC815-Y, 2SC2068, 2SC2331-Y)



	Forward Direction	Reverse Direction
Between B and E	Hundreds of ohms	Infinity
Between B and C	Hundreds of ohms	Infinity
Between E and C	Infinity	Infinity

● For PNP(KSA539-Y)



	Forward Direction	Reverse Direction
Between B and E	Hundreds of ohms	Infinity
Between B and C	Hundreds of ohms	Infinity
Between E and C	Infinity	Infinity

Alignment and Adjustments

3. IC (INTEGRATED CIRCUIT)

IC has built in DIODE against overvoltage in PIN. Generally, except for internal circuit defects, IC defects can be found, by measuring the DIODE.

Forward Direction	Hundreds of ohms
Reverse Direction	Varying depending on IC but generally normal
	Infinity in DIODE TEST MODE

✍ Defects have SHORT(0 ohm) for both forward and reverse direction.

MEMO

6. Circuit Description

6-1 Power supply

6-1-1 Outline(PDP SMPS)

Considering various related conditions, the switching regulator with good efficiency and allowing for its small size and light weight was used as the power supply for PDP 50inch, VS requiring high power consumption used forward converter and 12VSAMP used the simple flyback converter and other high voltage (VSCAN,VSET,VE)used DC/DC converter. To comply with the international harmonics standards and improve the power factor, active PFC(Power Factor Correction) was used to rectify AC input into +400V DC output, which in turns used as input to the switching regulator.

6-1-2 63"HD SMPS Specification

(1) Input

The PDP-PS-421S board should be designed so that the AC power supply within the 100VAC (common) to 150VAC and the input frequency within 50/60Hz can be applied.

(2) Output

The PDP-PS-421S board converts the AC Voltages (+165Vs1, +75Va, +185Ve, +5Vd, +12Vcc, +6Vsp, +9Vsp, +9Vcc, +12Vfan, +5Vd1, +5Va, +220Vset, +75Vscan, +18Vg) into the DC Voltages.
The usage and specification of each output is as shown in Table 1.
Table 1 shows the power supplies for PDP SMPS.

Table1. Specifications of Output Power Supplies for PDP SMPS

Output Voltage (V)	Voltage Setting (Normal Load)	Output Voltage Variable Point	Output Current(A)		
			Min	Non	Max
165Vs	165V ± 1%	160V ~ 190V	0.2	2.0	0.2
75Va	75V ± 1%	60V ~ 85V	0.2	2.0	0.2
185Ve	185V ± 1%	170V ~ 200V	0.01	0.1	0.01
220Vset	220V ± 1%	200V ~ 250V	0.01	→	0.01
75Vscan	75V ± 1%	60V ~ 90V	0.01	→	0.01
5Vd	5.2V ± 1%	4.5V ~ 5.5V	0.3	→	0.3
18Vg	18V ± 5%	-	0.07	→	0.07
5Vdl	5.2V ± 1%	4.5V ~ 5.5V	0.2	→	0.2
5Va	5.2V ± 1%	-	0.1	→	0.1
9Vcc	9.2V ± 5%	-	0.07	→	0.07
12Vcc	12.2V ± 5%	-	0.07	→	0.07
6Vsp	6V ± 5%	3V ~ 24V	0.25	2.5	0.25
12Vfan	11V ~ 14V	-	0.1	→	0.1
5Vsb	5.2V ± 1%	5.0V ~ 5.4V	0.1	1.0	0.1

Table 2. Security function SPEC required for PDP SMPS

Division	OCP Current	OVP Voltage	UVP Voltage	Short Circuit
+165Vs	5 ~ 7A	190 ~ 220V	135 ~ 145V	OK
+ 75Va	3 ~ 4A	85 ~ 100V	50 ~ 65V	OK

(3) FUNCTION OF BOARD

1) Remote control

Using 120V / 10A relay, the board makes remote control available.

2) Voltage

The board designed so that input voltage can be used within 100 VAC to 150VAC.

3) Improvement of power factor

The board is designed using PFC circuit so that PF (Power Factor) can be over 0.95, because low PF can be a problem in high voltage power.

4) Protection

The OCP (Over Current Protection), the OVP (Over voltage Protection), and the Short Circuit Protection functions are added against system malfunction.

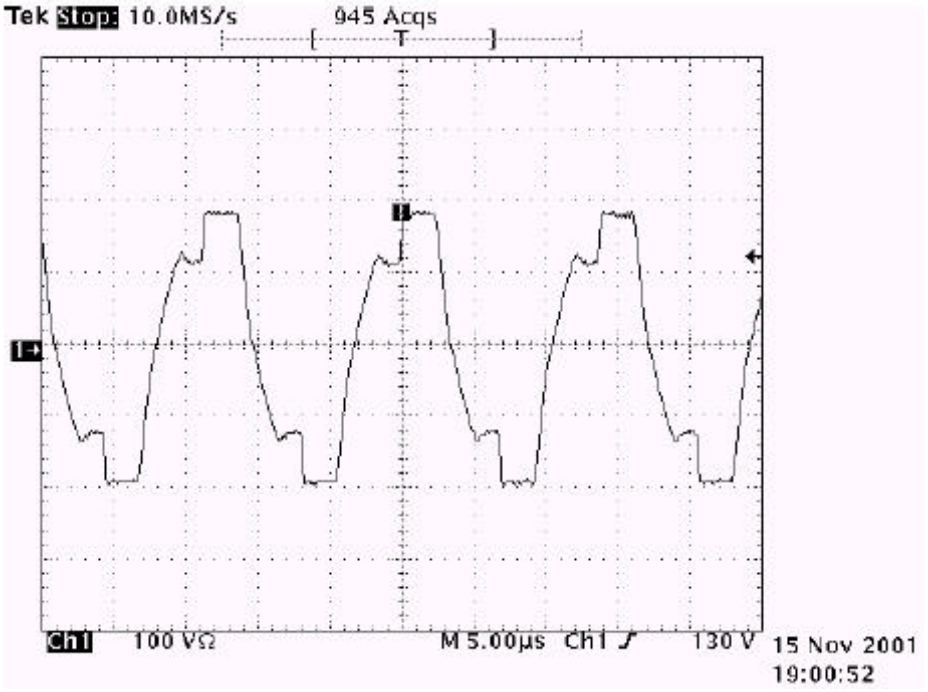
(4) BLOCK DIAGRAM

This product can be defined as a power supply device (Input power: AC110 / 220V), consists of Inrush Current Limit Circuit on Input and Power Factor Correction circuits, VS, VA, and VI Block, providing the power (current) required for PDP Panel discharges and external circuits. PFC circuit utilizes Discontinuous Current Mode (DCM) that produces a high efficiency. And, an input EMI filter circuit is equipped on the exterior.

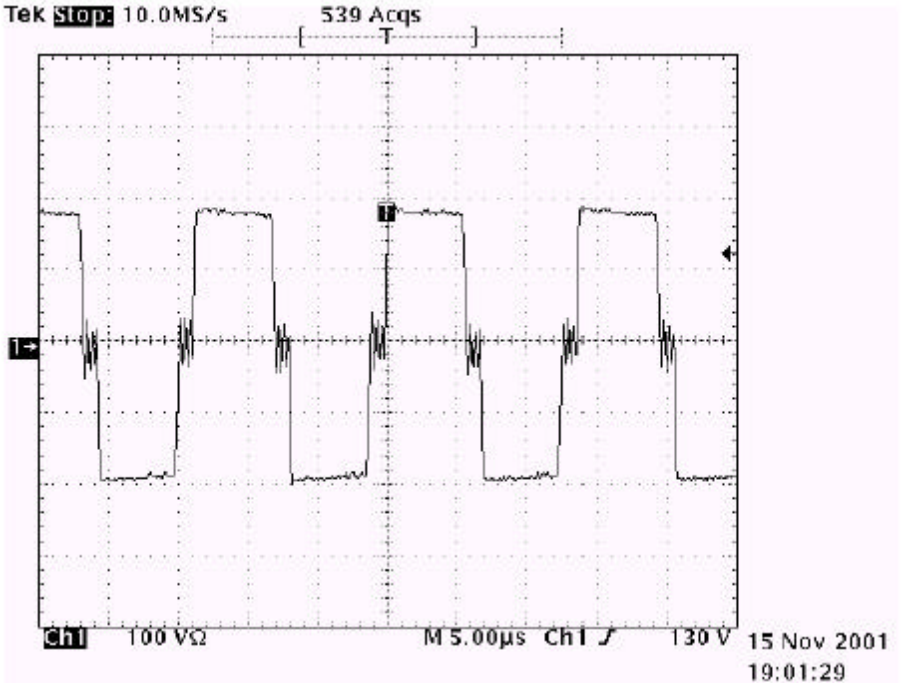
1) PFC Block Boost Discontinuous Current Mode (DCM) PFC circuit is used for PFC (Power Factor Correction), where a common PWM IC gives an easy control, a simple circuit onfiguration, and a high efficiency. The circuit operates as described as following:RELAY is to be operated by inputting initial Relay “ON” while the resistance for Inrush Current Limit charges a capacitor of PFC Output Terminal. If the charged voltage of the capacitor goes over 340V, a comparator of PFC circuit controller activates VA Block and Relay for Inrush Current Limit. Thereafter, PFC circuit initiates a normal operation.

PFC circuit has output, voltage, current limit circuits for placing a restriction on switching current, and protective (safeguard) circuits against output over-voltage. The over-voltage induces input Terminal Relay to be “OFF” with the set shut down.

2) Vs Block supplies the sustain power closely related to PDP Panel and includes 165Vs and 185Ve employing a Full-bridge circuit as Topology. In order to insulate gate signal, Driver at the secondary side based on properties of the pulse type of load. 185Ve power utilizes a variable Regulator for sub-output of 165Vs power, which is supplied to the load being added to 165Vs power. 70kHz is applied for switching frequency that has the Sequence operated after rising 5Vd power.

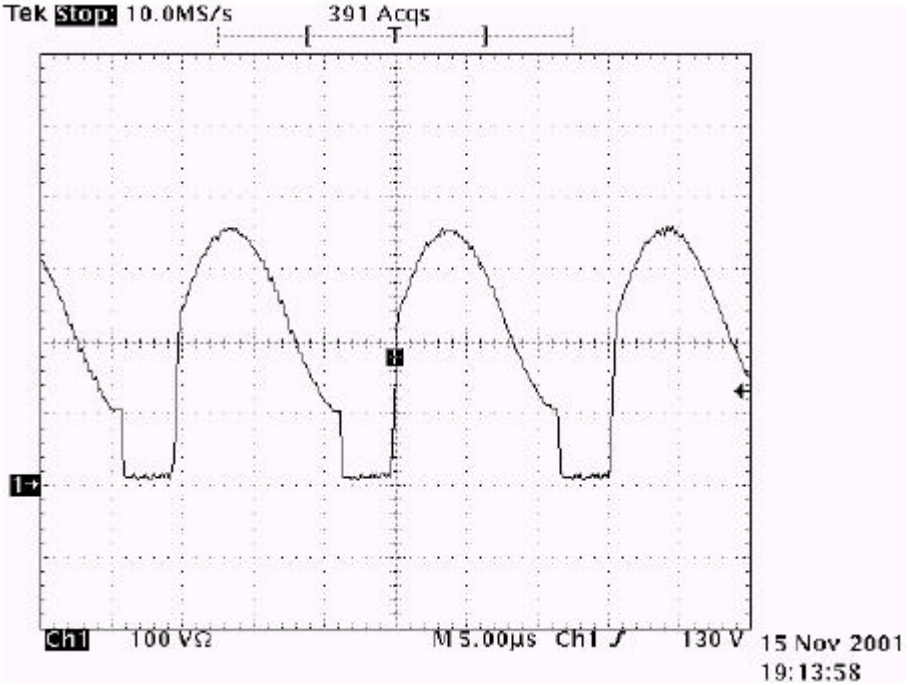


Vs Switching Pulse(Pulse for power board operation only)



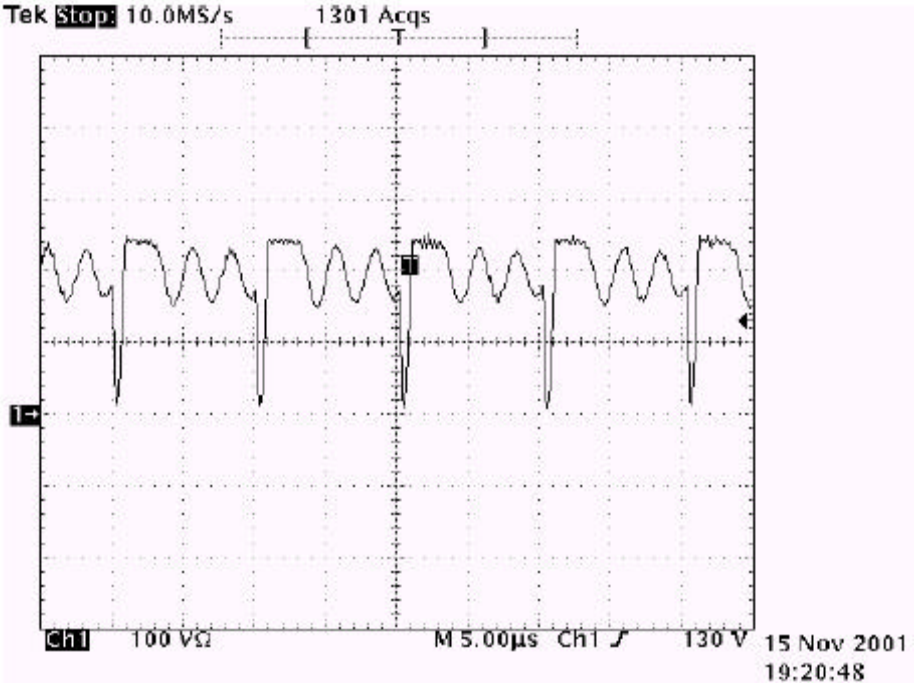
Va Switching Pulse(Pulse for Set ON)

3) Va Block Va Block consists of address voltage suppliers (75Va, 220Vset, and 75Vscan), VCCs that supply a power to logic circuit, and 12V fan; the power of cooling Fan of 18Vg. PDP Set that provides Gate voltages of drive circuit. It utilizes a Forward circuit mode as TOpology. 75Vscan uses 75Va power to construct not only stable but, if needed, also variable DC/DC Converter while 220Vset, also variable if wanted, is applied by adding 165Vs power to the power generated from Buck Converter with 75Va power. 5Vd and 12Vsp power can be generated by Buck Converter with the power gained through Coupling in Transformer, and 18Vg by Linear Regulator. The switching frequency is 70kHz.

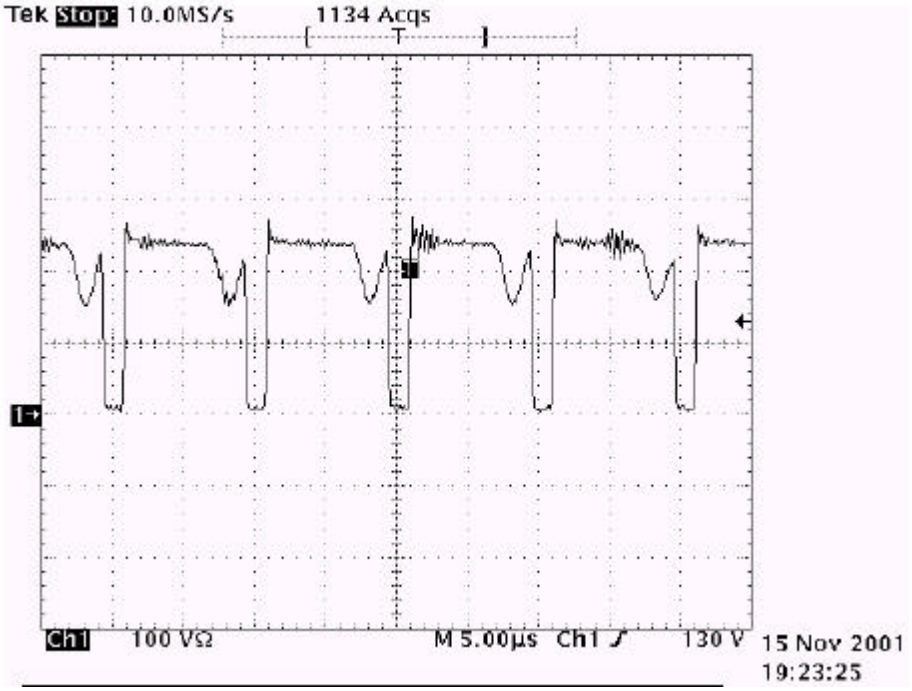


Va Switching Pulse(Pulse for Set ON)

4) Block VI Block consists of voltage suppliers for image circuits (5Va, 9Vcc, 12Vcc, and 5Vd1), and a Flyback circuit mode is applied as Topology. Feedback for voltage stability is designed for 5Vd1, 5Va, 9Vcc, 12Vcc, and 5Vd1 powers anr generated by using each Linear Regulator for the power gained through Coupling in Transformer. The switching frequency is 100kHz.



VI Switching Pulse(Pulse for power board operation only)



VI Switching Pulse(Pulse for Set ON)

6-1-3 Pin Assignment

Image Board

NO	OUTPUT	LOC
1	+5V	VSB
2	GND(D)	
3	GND(D)	
4	+5V	V5(D)
5	RELAY	
6	THDET	
7	FAN	
8	GND	
9	GND	
10	N.C	
11	+12V	V12
12	+5V	V5(D)
13	N.C	

SX(X Driver)

NO	OUTPUT	LOC
1	+5V	V5(D)
2	GND	
3	+18V	VG
4	GND	
5	70V	VSCAN
6	GND	
7	230V	
8	N.C	
9	GND	
10	GND	
11	165V	VS
12	165V	VS
13	165V	VS

SY(Y Drive)

NO	OUTPUT	LOC
1	+5V(D)	V5(D)
2	GND(D)	
3	+18V	VG
4	GND	
5	200V	VE
6	GND	
7	70V	VSCAN
8	GND	
9	GND	
10	165V	VS
11	165V	VS
12	165V	VS

Speaker

NO	OUTPUT	LOC
1	+5V	
2	GND	
3	+9V	V9
4	+12V	V12
5	GND	
6	+6V	VSAMP
7	+6V	VSAMP
8	GND	
9	GND	

Buffer(2EA)

NO	OUTPUT	LOC
1	+70V	VA
2	+70V	VA
3	GND	
4	GND	

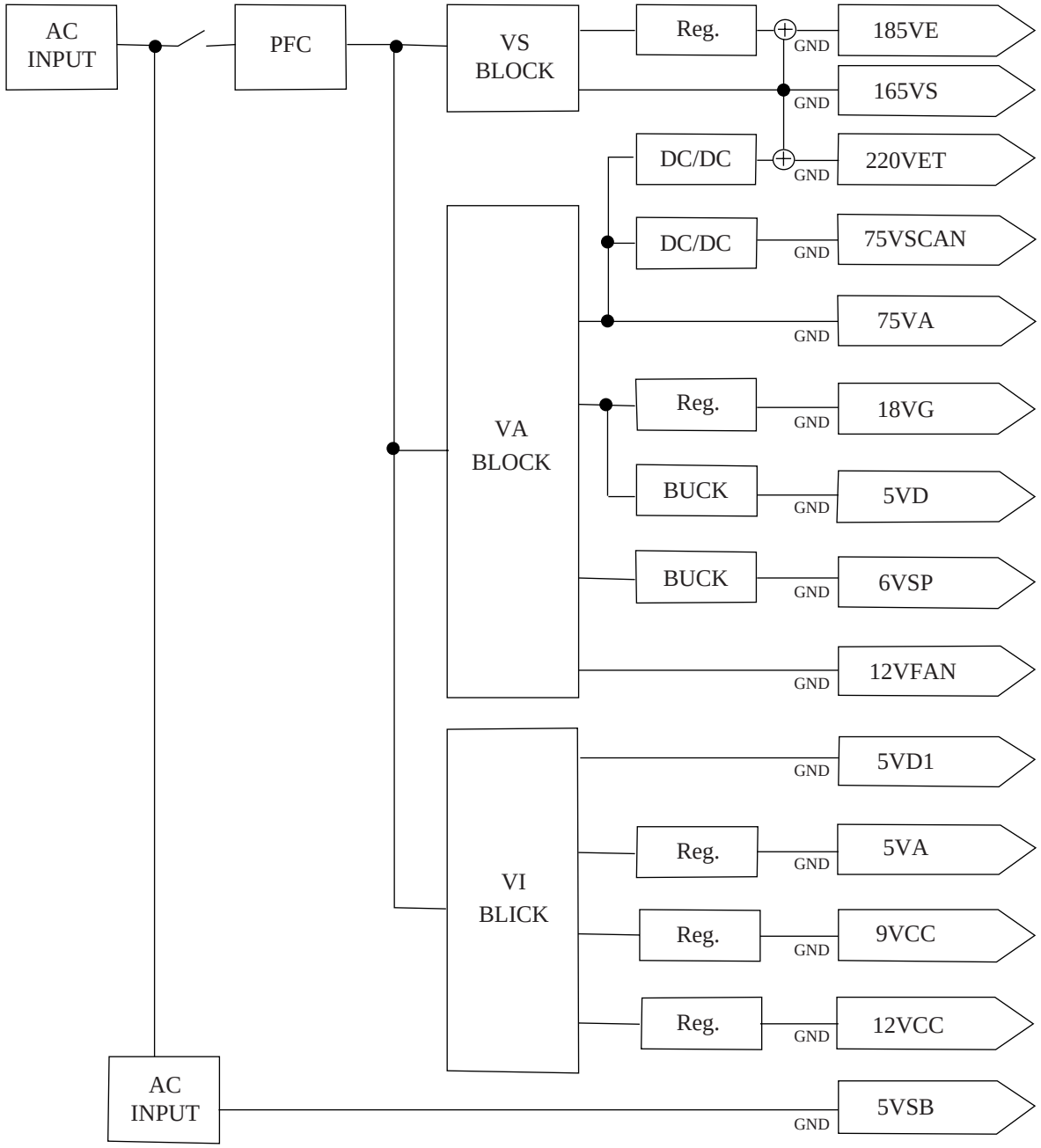
Fan(3EA)

NO	OUTPUT	LOC
1	+12V	VFAN
2	GND	

SL(Logic)

NO	OUTPUT	LOC
1	+70V	
2	+70V	
3	GND	
4	GND	

6-1-4 SMPS Block diagram



6-2 Driver circuit

6-2-1 Driver circuit overview

6-2-1(A) WHAT IS THE DRIVER CIRCUIT

It is a circuit generating an appropriate pulse (High voltage pulse) and then driving the panel to implement images in the external terminals (X electrode group, Y electrode group and address electrode), and this high voltage switching pulse is generated by a combination of MOSFETs.

6-2-1(B) PANEL DRIVING PRINCIPLES AND TYPES OF DISCHARGE BY DRIVE PULSE

In PDP, images are implemented by impressing voltage on the X electrode, Y electrode and address electrode, components of each pixel on the panel, under appropriate conditions. Currently, ADS (Address & Display Separate: Driving is made by separating address and sustaining sections) is most widely used to generate the drive pulse. Discharges conducted within PDP pixels using this method can largely be classified into 3 types, as follows:

① Address discharge: This functions to generate wall voltage within pixels to be lighted by addressing information to them (i.e., impressing data voltage)

② Sustaining discharge: This means a display section where only pixels with wall voltage by the address discharge display self-sustaining discharge by the support of such wall voltage. (Optic outputs realizing images are generated.)

③ Ramp reset discharge: To have address discharge occur selectively in pixels, all pixels in the panel must have the same conditions (i.e., the same state of wall and space electric discharges). The ramp reset discharge section, therefore, is important to secure the drive margin, and methods most widely used to date include wall voltage controlling by ramp pulse.

6-2-1(C) Discharge of Drive

① Sustaining discharge

1(C). Kinds and detailed descriptions of driving discharge
Sustaining discharge means a self-sustaining discharge generated by the total of the sustaining pulse voltage (usually, 160~180V) alternately given to X and Y electrodes during the sustaining period and the wall voltage which varies depending upon pixels' previous discharge status. It is operated by the memory function (through this, the current status is defined by previous operation conditions) AC PDP basically possesses. That is, when there is existing wall voltage in pixels (in other words, when pixels remain ON), the total of wall voltage and a sustaining voltage to be impressed subsequently impresses a voltage equal to or above the discharge start voltage, thereby generating discharge again, but when there is no existing wall voltage in pixels (in other words, when pixels remain OFF), the sustaining voltage only does not reach the discharge start voltage, thus causing no discharge. The sustaining discharge is a section generating actual optic outputs used in displaying images.

② Address discharge

This means a discharge type generated by the difference between positive voltage of the address electrode (usually, 60~70V) and GND of the Y electrode. The address discharge serves to generate wall voltage in pixels where images are to be displayed (that is, discharge is to be generated) prior to the sustaining discharge section. Namely, pixels with wall voltage by the address discharge will generate sustaining discharge by the following sustaining pulses.

③ Weak erasing discharge

The purpose of resetting discharge is to make even wall voltage in all pixels on the panel.
Wall voltage which may vary depending upon the previous sustaining discharge status must be made even. That is, wall voltage generated by the sustaining discharge must surely be removed, by making discharges and then supplying ions or electrons. Wall voltage can be removed by making discharges and then setting a limitation on time for opposite polarity charging of the wall voltage or generating weak discharge (Low voltage erasing) to supply an appropriate quantity of ions or electrons and keep polarities from being charged oppositely. The weak discharge (Low voltage erasing) methods which have been known to date can largely be into two types:

1) the log pulse adopted by most companies including F Company, and
2) the ramp pulse adopted by Matsushita.

In both two methods, impression is made with a slow rising slope of the erasing pulse. Because the total of the existing wall voltage and a voltage on the rising pulse must be at least the drive start voltage to generate discharges, external impressed voltage is adjusted based on the difference in wall voltage between pixels.
And, weak discharge is generated because of a small impressed voltage.

6-2-2 Driver Circuit Block Diagram

(1) Y

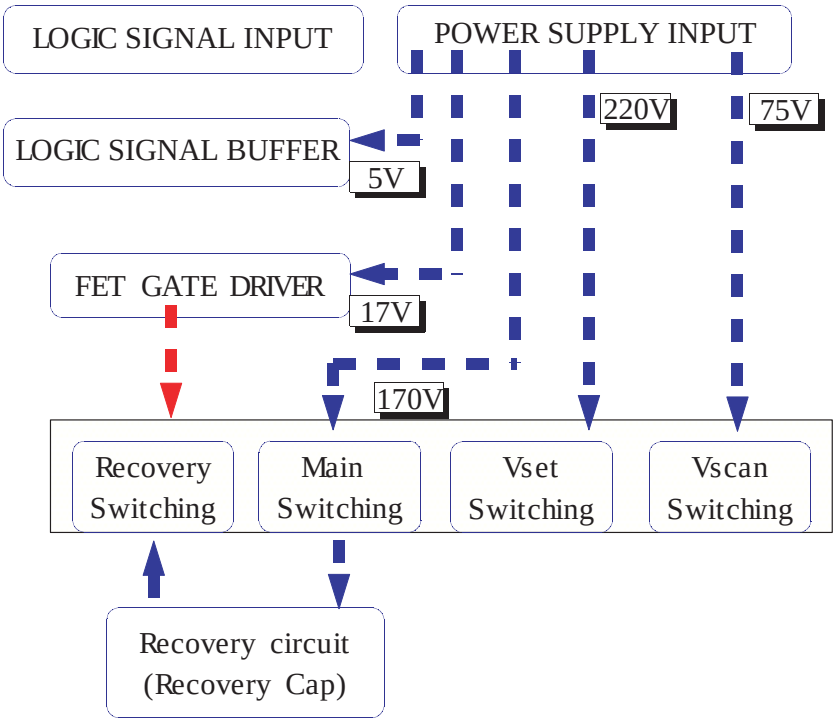


Fig. Driver Y-Bd

(2) X

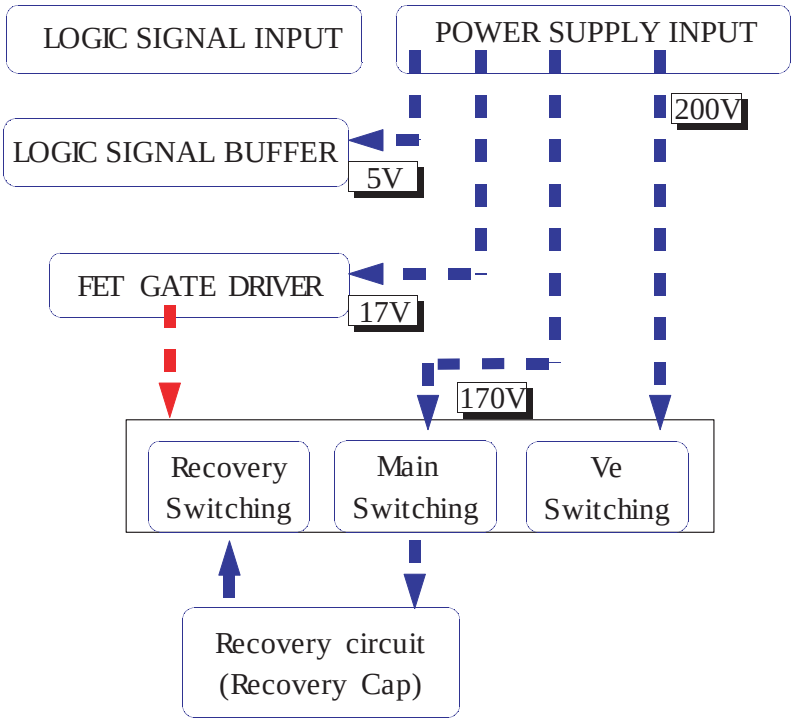


Fig. Driver Y-Bd

(3) Key Requirements of the Driver Circuit Operations

1) Power Supply

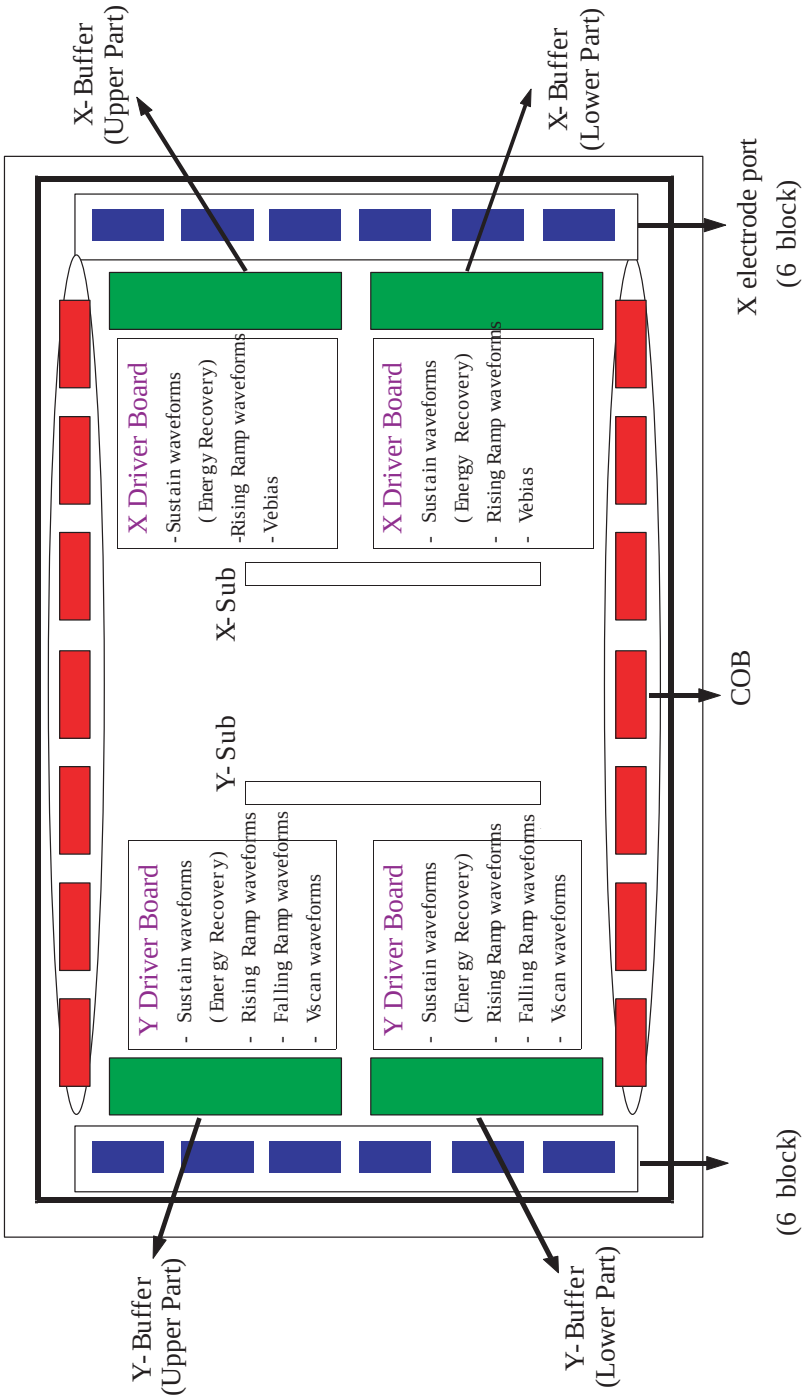
- Power is supplied from the power board. The minimum value may differ from the following.

2) Logic Signals

- Logic signals are supplied from the logic board.
- Gate signals of each FET

(4) Diagram and Functional Description of the Driver Circuit

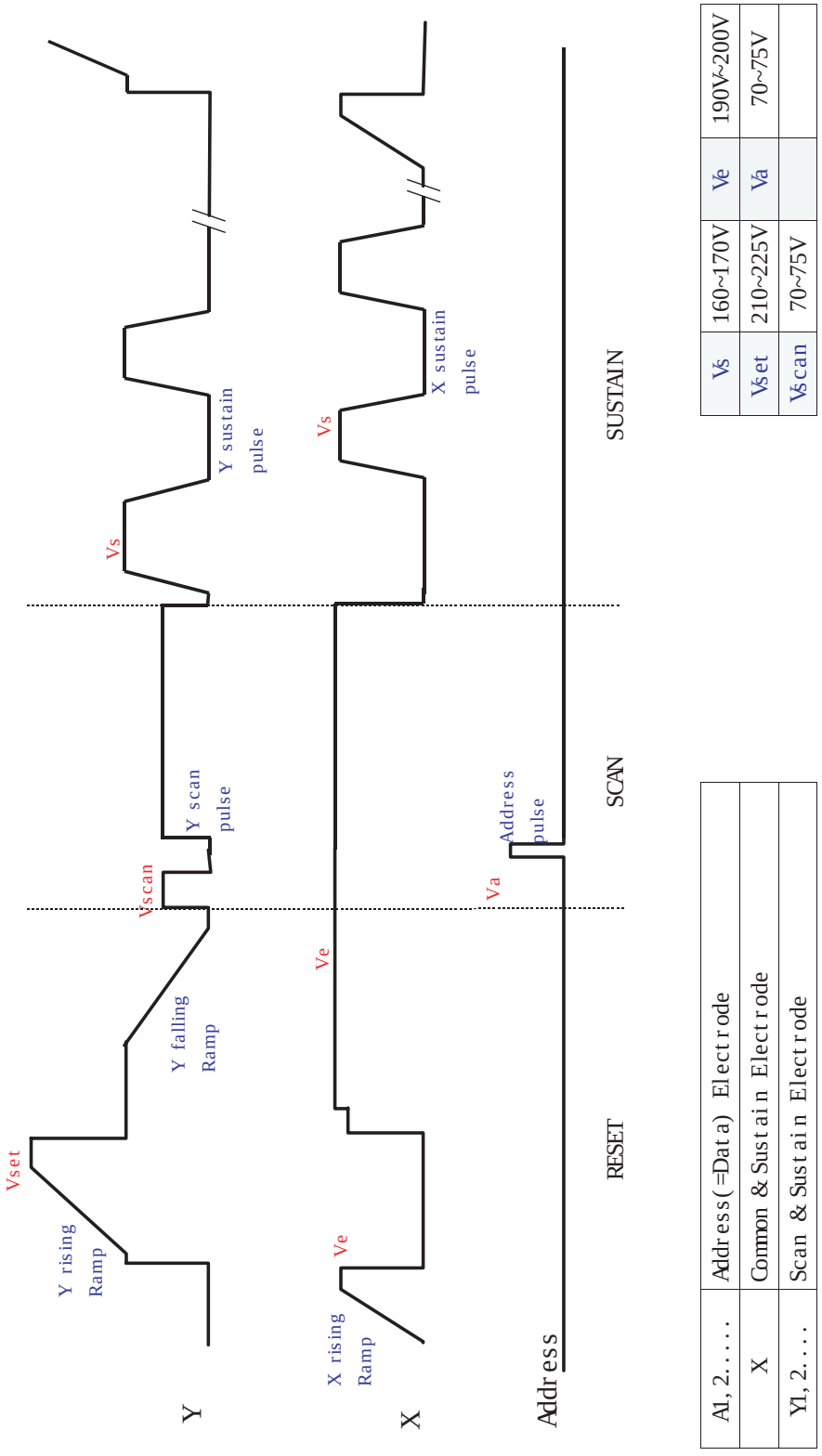
- Functional Description of Each Board



1) X Board I, II
   X Board I and II are connected to the X port on the panel to:
   - Produce sustain voltage waveforms (including ERC)
   - Produce X rising ramp waveforms
   - Sustain Ve bias during the Scan.
2) Y Board I, II
   Y Board I and II are connected to the Y port on the panel to:
   - Produce sustain voltage waveforms (including ERC)
   - Produce Y rising ramp waveforms
   - Sustain V scan bias.
3) X Buffer Board (Upper and Lower)
   The X buffer board applies Sustain waveforms to the X port. It consists of an upper and a lower board.
4) Y Buffer Board (Upper and Lower)
   The Y buffer board applies Scan waveforms to the Y port. It consists of an upper and a lower board. Each board is installed with 6 Scan driver ICs (STMicroelectronics STV7616: 64 or outputs).
5) X Sub Board
   The X sub board distributes and applies logic data to the X board I and II.
6) Y Sub Board
   The Y sub board distributes and applies logic data to the Y board I and II.
7) COB
   The COB applies Va waveforms to the Address electrodes during the Address stage to produce Address discharges by using the difference between the injection waveforms and the voltage applied to the Y electrode. A COB is installed with 4 data drive ICs (STMicroelectronics STV7610A: 96 outputs). A total 22 COBs are required.

6-2-3 Driving Waveform Specs

6-2-3(A) Driving Waveform Diagram



A1, 2.....	Address(=Data) Electrode
X	Common & Sustain Electrode
Y1, 2....	Scan & Sustain Electrode

Vs	160~170V	Ve	190V~200V
Vset	210~225V	Va	70~75V
Vscan	70~75V		

6-2-3(B) Functional Description of Each Waveform

(1) X Rising Ramp Waveform

The last Y electrode Sustain waveform is applied from the sub field before the XZ Rising Ramp waveforms begin to be applied. The last waveform triggers the Sustain Discharge.
Then, a positive wall charge occurs on the X electrodes and a negative wall chanrge on the Y electrodes.
The X rising ramp eliminates the wall charge produced by the aforementioned Sustain Discharge waveform by triggering a low discharge.

(2) Y Rising Ramp Waveform

During the Y Rising Ramp stage, an external voltage of 390-400V is applied to the Y electrodes to adjust each Gap Voltage to the same initial voltage level before starting a low discharge. As the low discharge is sustained, a negative wall charge continues on the Y electrodes and a positive wall charge on the X and Address electrodes across the panel.

(3) Y Falling Ramp Waveform

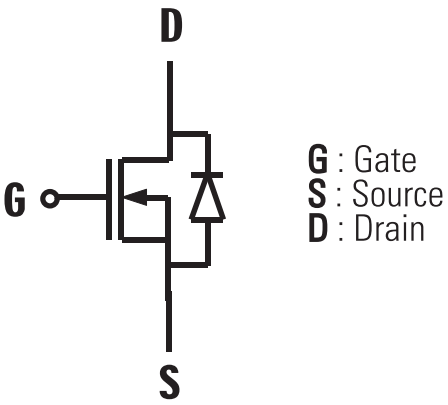
During the Y Falling Ramp stage, most of the negative wall charges on the Y electrodes, with approximately 200V X bias, are used to eliminate the positive wall charges on the X electrodes. Most of the positive wall charges on the (OV) rising ramp section of the Address electrodes are sustained to form wall charges in preparation for an address discharge.

(4) Y Scan Wavdform

The Y Scan waveform is also calle an injection waveform. It selects Y electrodes one line at a time. Vscan is referred to as Scan bias voltage. About 70 Volts (V scan)are applied to the applicable electrode limes with Vscan, and 0 Vots (GND) to the rest. When Ramp waveforms are applied, however, a negative wall charge occurs on the Y electrodes, and a positive wall charge on the Address electrodes. Because the voltage level exceeds the initial discharge level in those cells affected by address waveforms (70~75V), an address discharge occurs. The PDP Address takes a long time because it applies injection and data waveforms line by line.

6-2-3(C) Principles of Fets Operation and High Voltage Switching

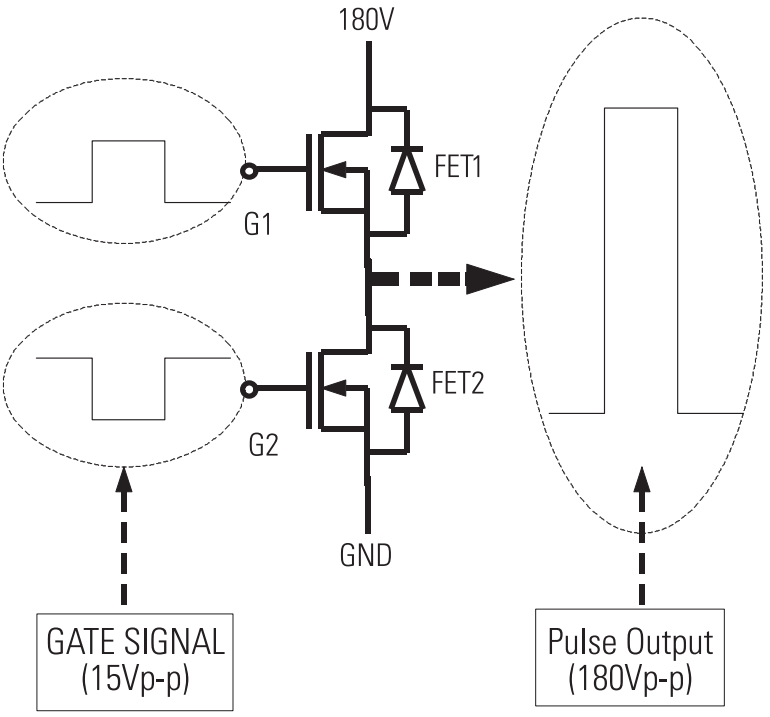
■ FET's operation principles



1) With signal impressed on the gate(Positive voltage) , FET gets short-circuited (a conducting wire of zero (0) resistance); and

2) With no signal impressed on the gate (GND), FET gets open-circuited (a non-conducting wire of ∞ resistance).

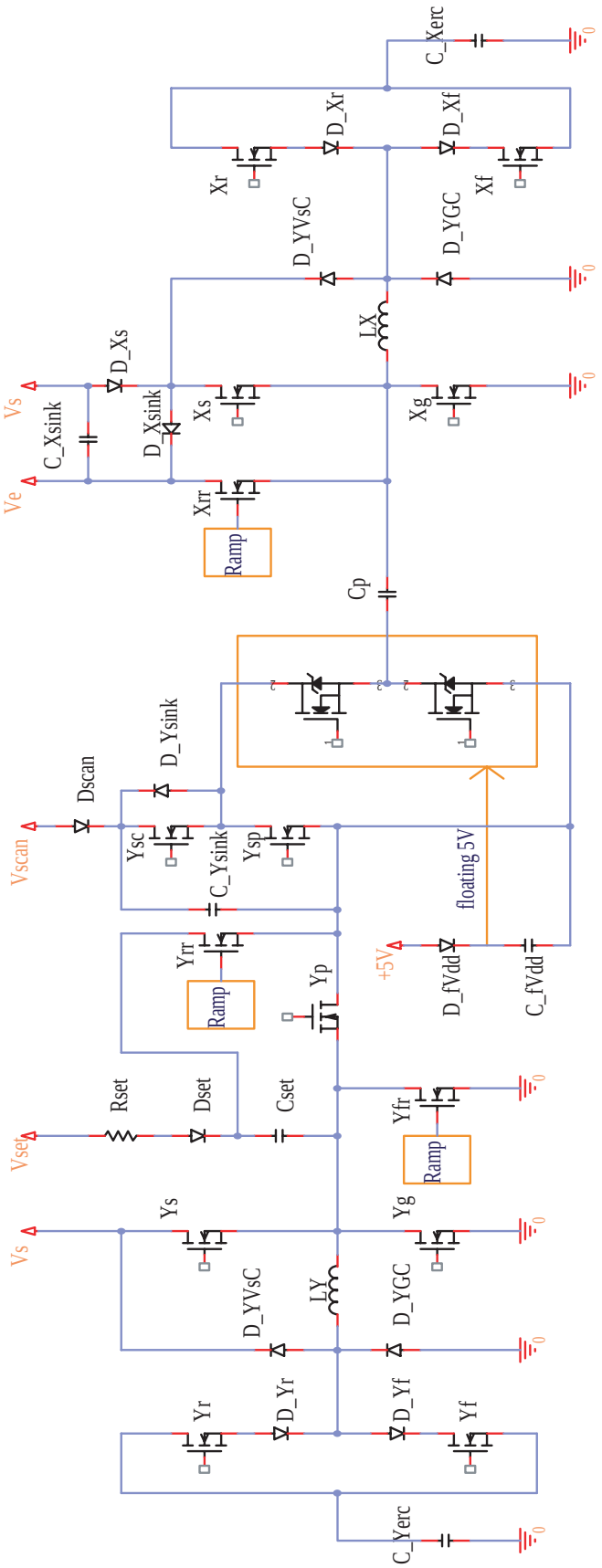
■ FET's high voltage switching principles



1) With no signal impressed on G1, FET1 gets open-circuited, and with signal impressed on G2, FET2 gets short-circuited, thereby causing GND to be outputted to output terminals.

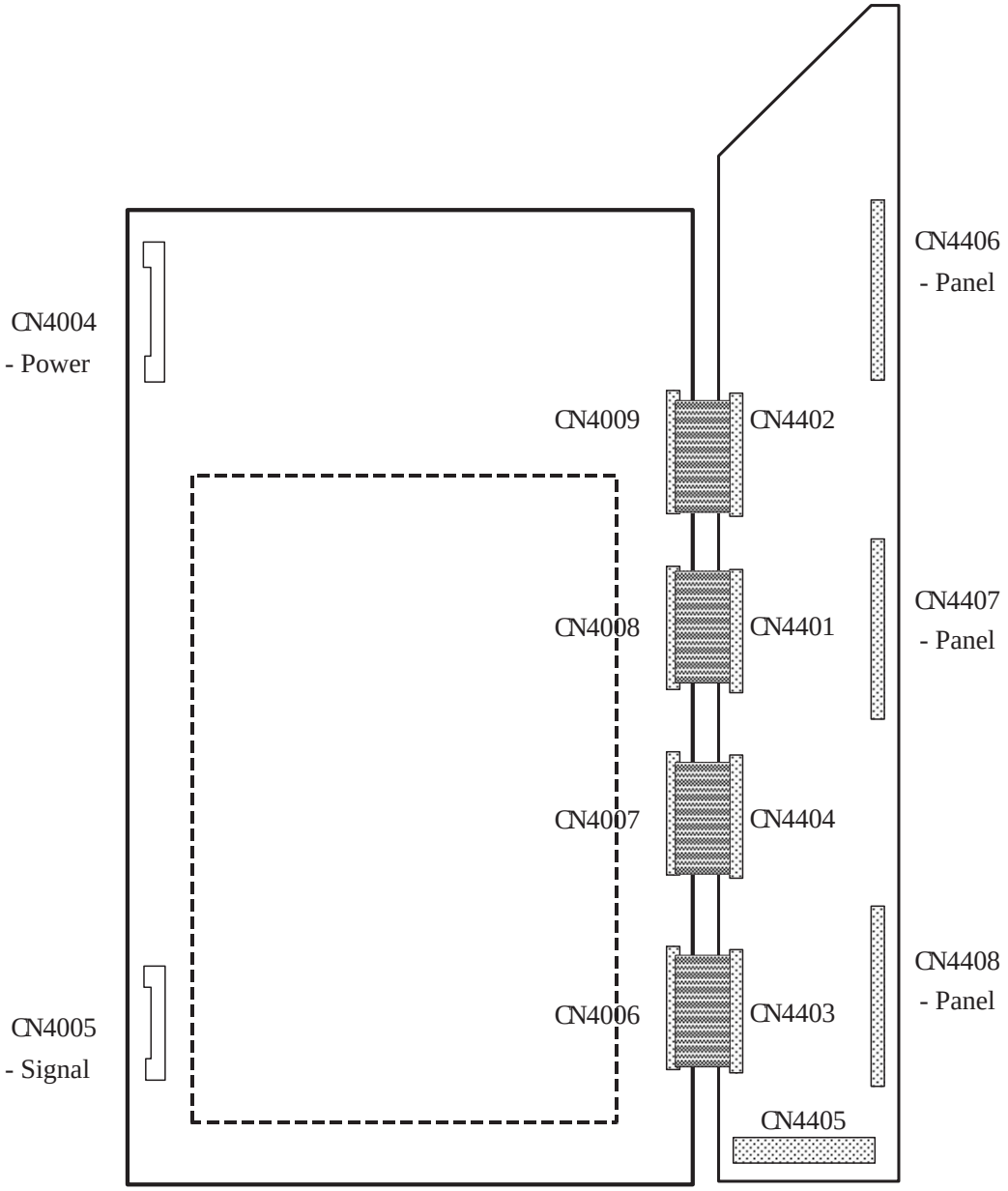
2) With signal impressed on G1, FET1 gets short-circuited, and with no signal impressed on G2, FET2 gets open-circuited, thereby causing 180V to be outputted to output terminals.

6-2-3(D) Driver Circuit Composition Diagram

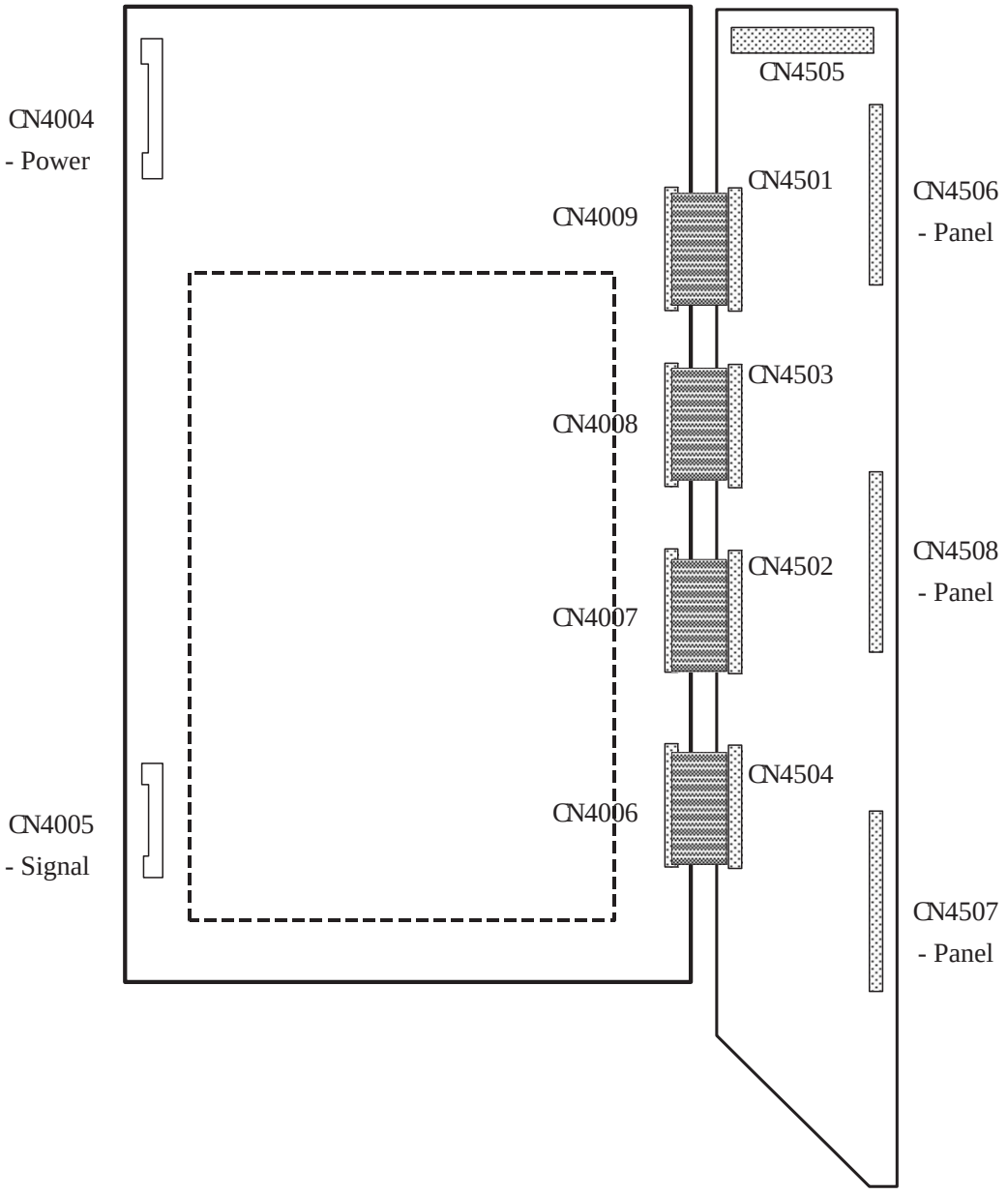


6-2-3(E) Driver Board Connector Layout

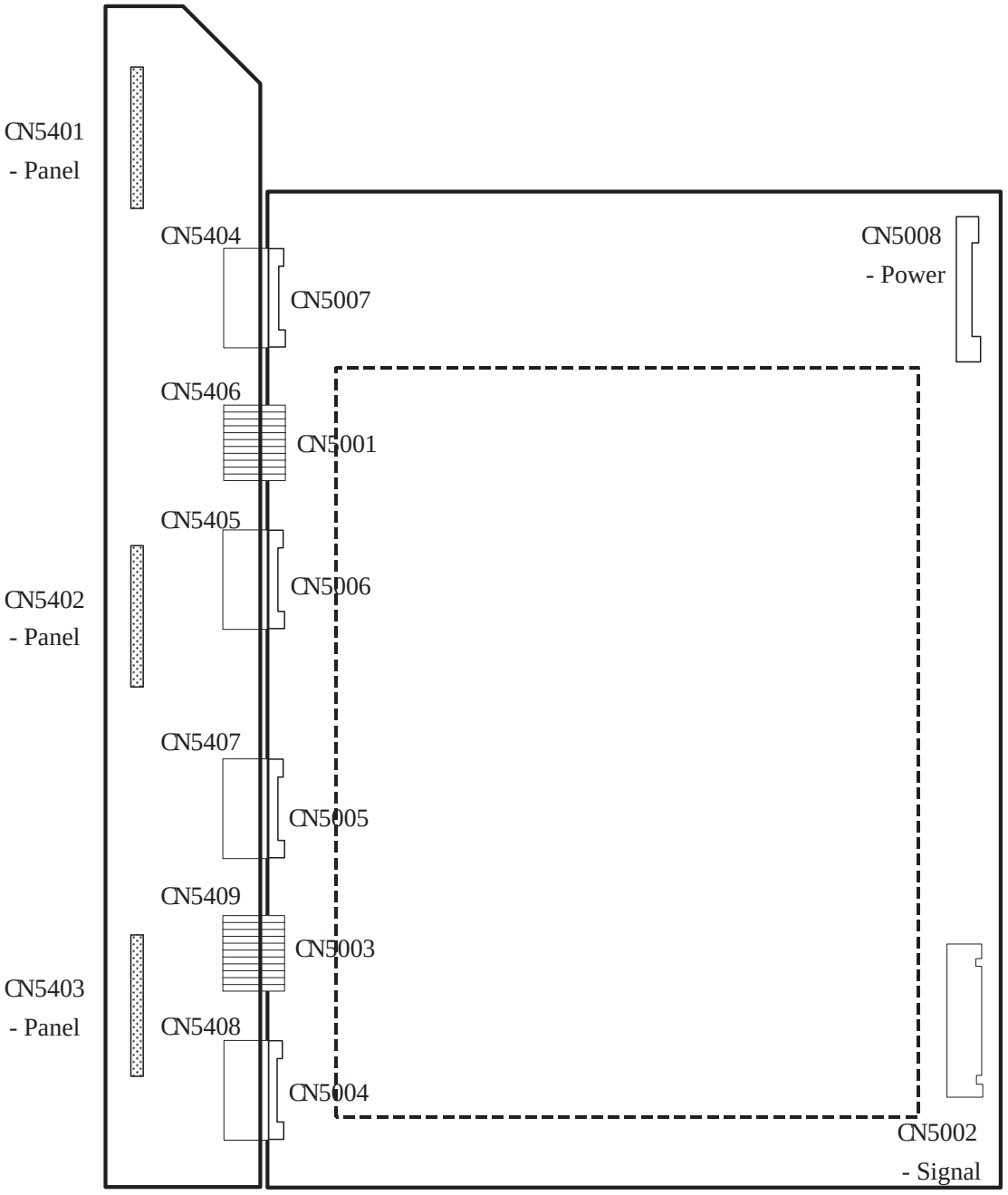
(1) X I



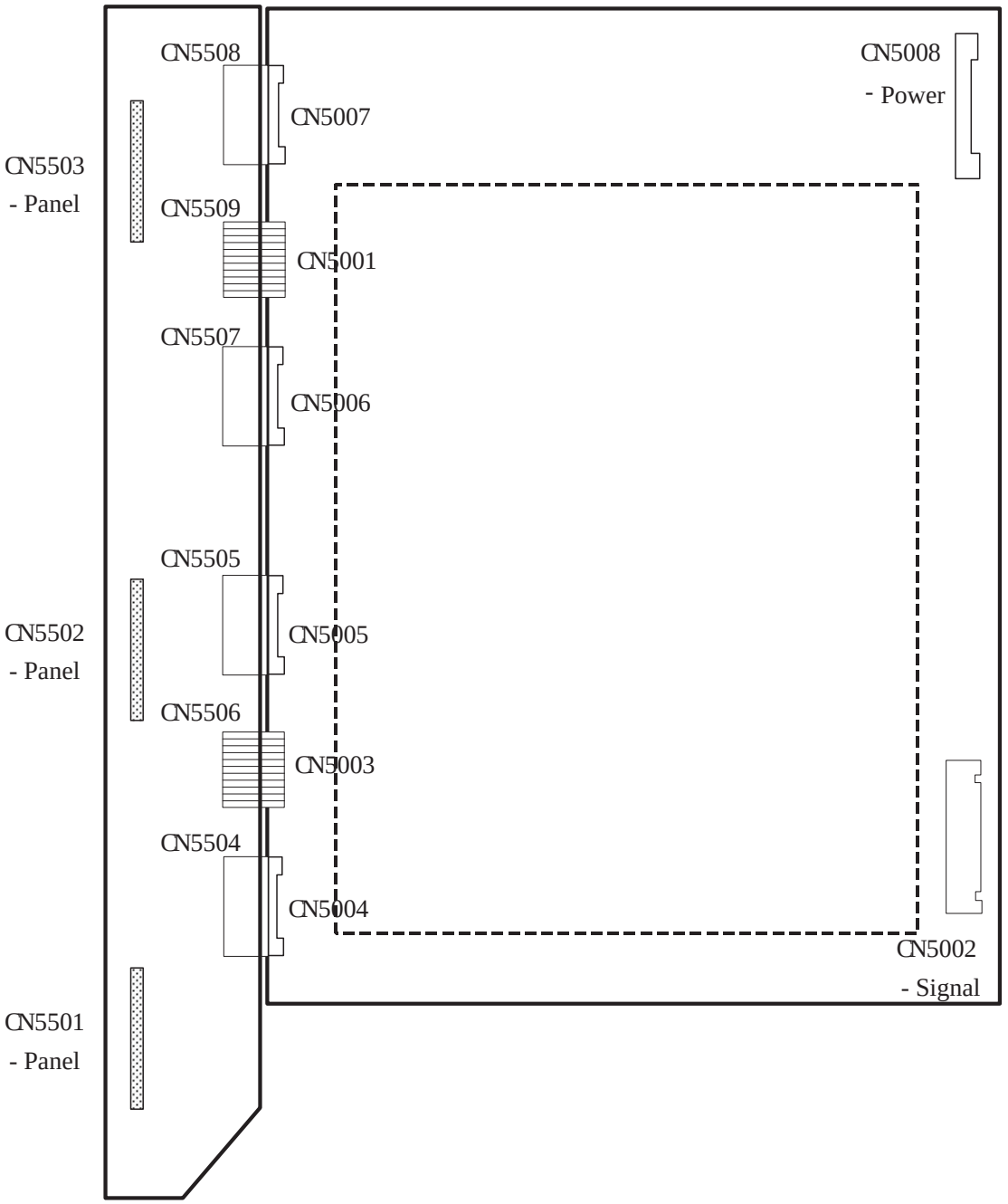
(2) X II


CN4004
- Power
CN4005
- Signal
CN4009
CN4008
CN4007
CN4006
CN4505
CN4501
CN4503
CN4502
CN4504
CN4506
- Panel
CN4508
- Panel
CN4507
- Panel

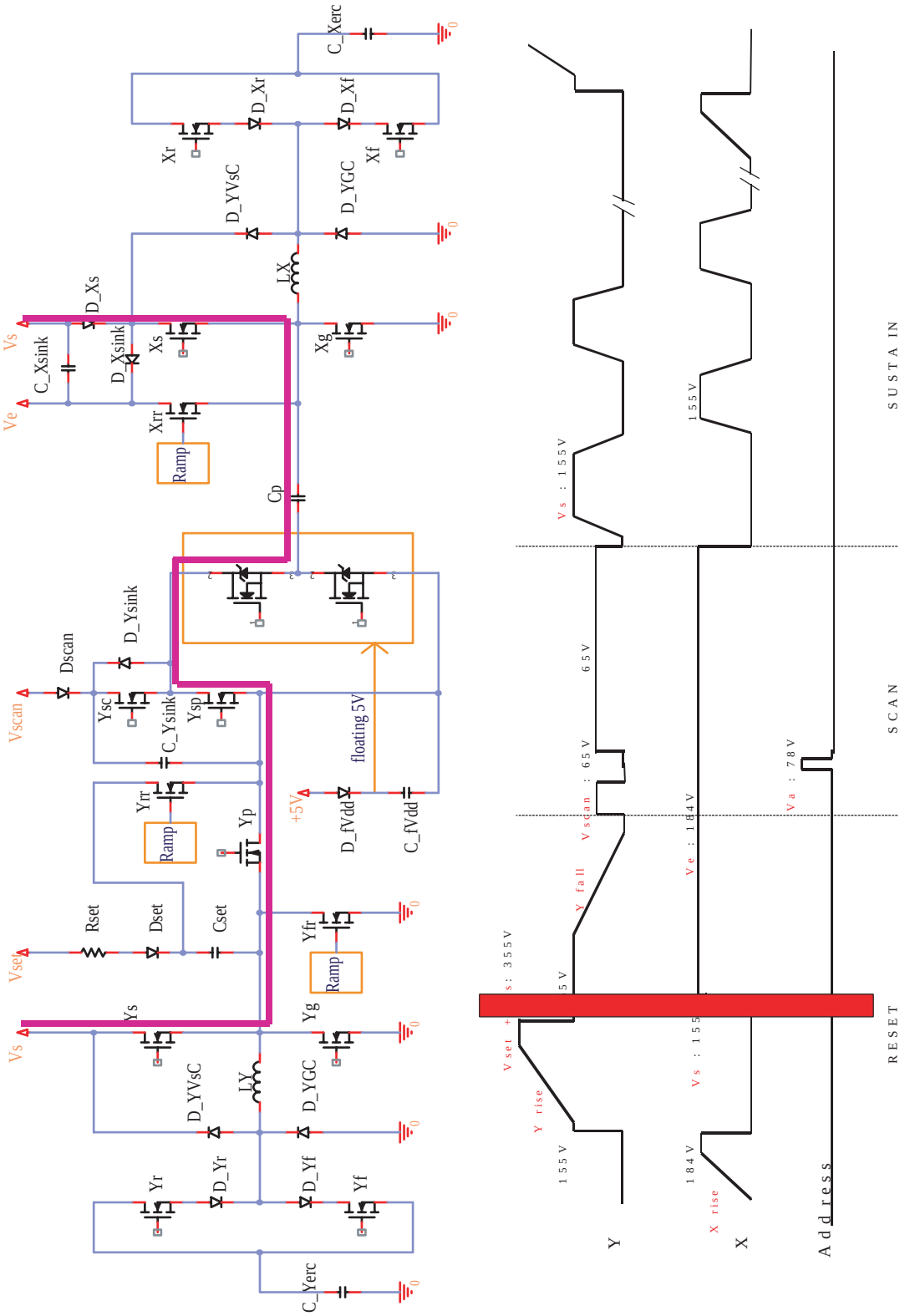
(3) Y I


CN5401
- Panel
CN5404
CN5007
CN5008
- Power
CN5406
CN5001
CN5405
CN5006
CN5402
- Panel
CN5407
CN5005
CN5409
CN5003
CN5403
- Panel
CN5408
CN5004
CN5002
- Signal

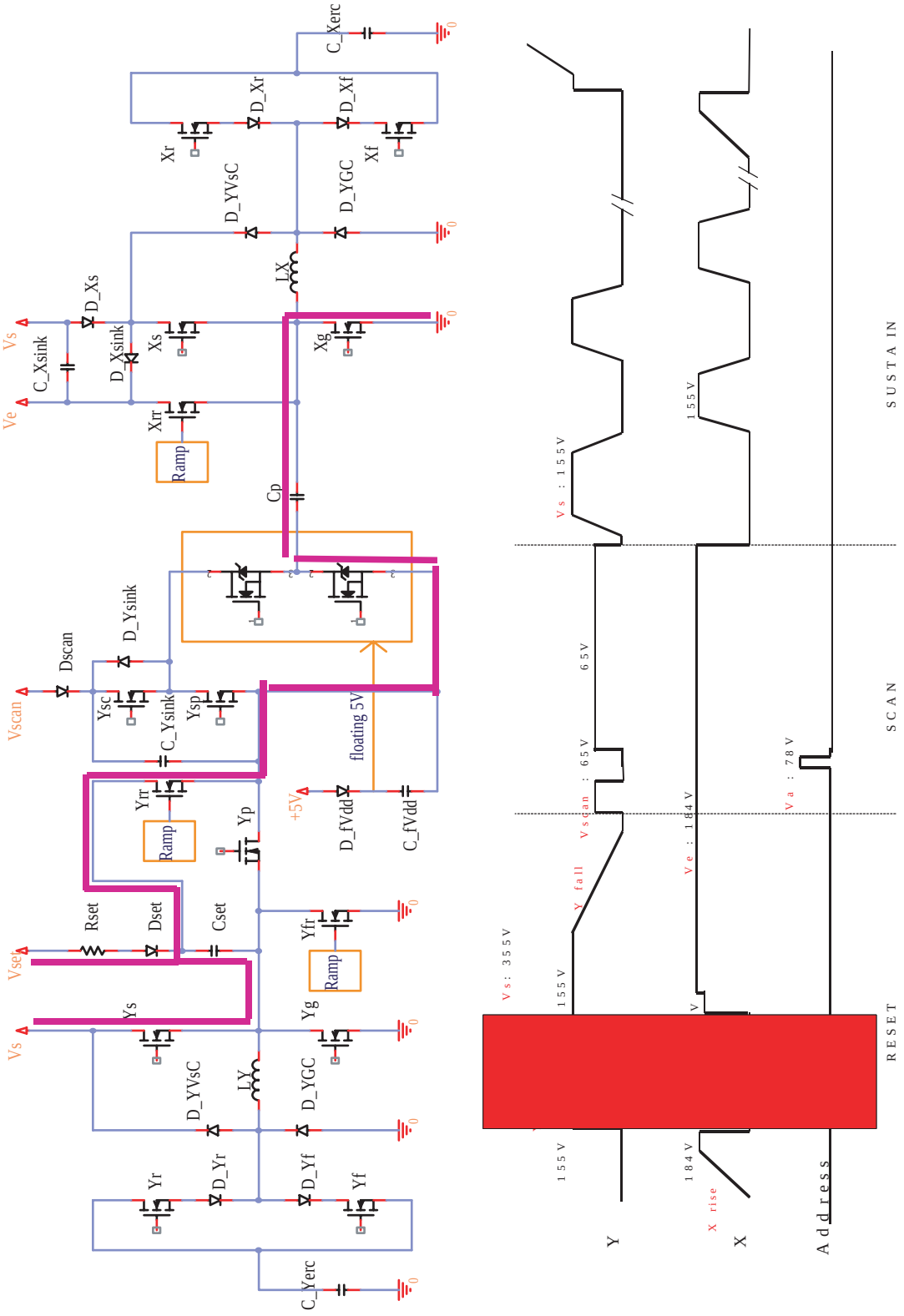
(4) Y II


CN5508
CN5007
CN5008
- Power
CN5503
- Panel
CN5509
CN5001
CN5507
CN5006
CN5505
CN5005
CN5502
- Panel
CN5506
CN5003
CN5504
CN5004
CN5002
- Signal
CN5501
- Panel

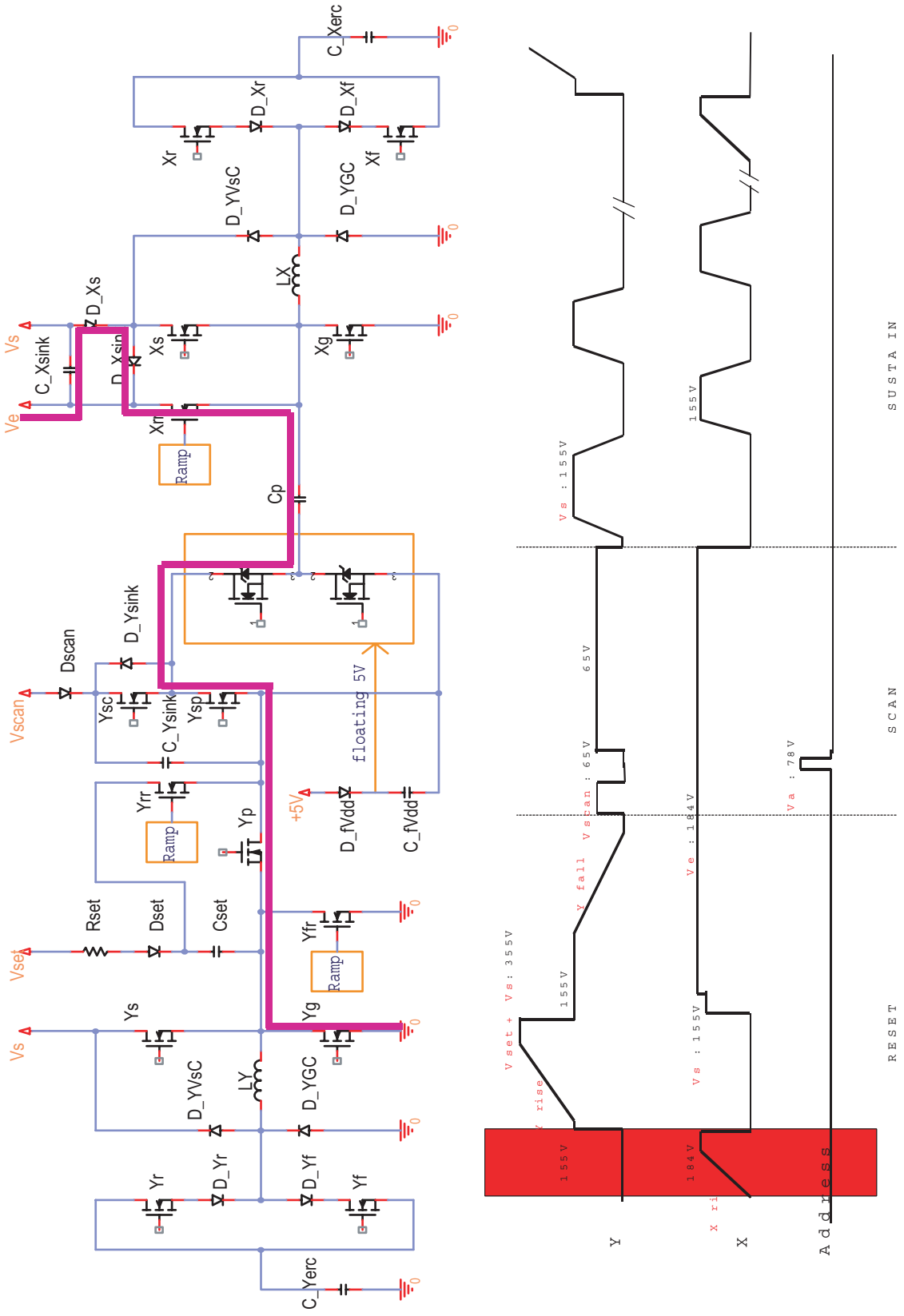
Single scan mode PDP action : Rest section, X : 0 -> Ve, Y : 0



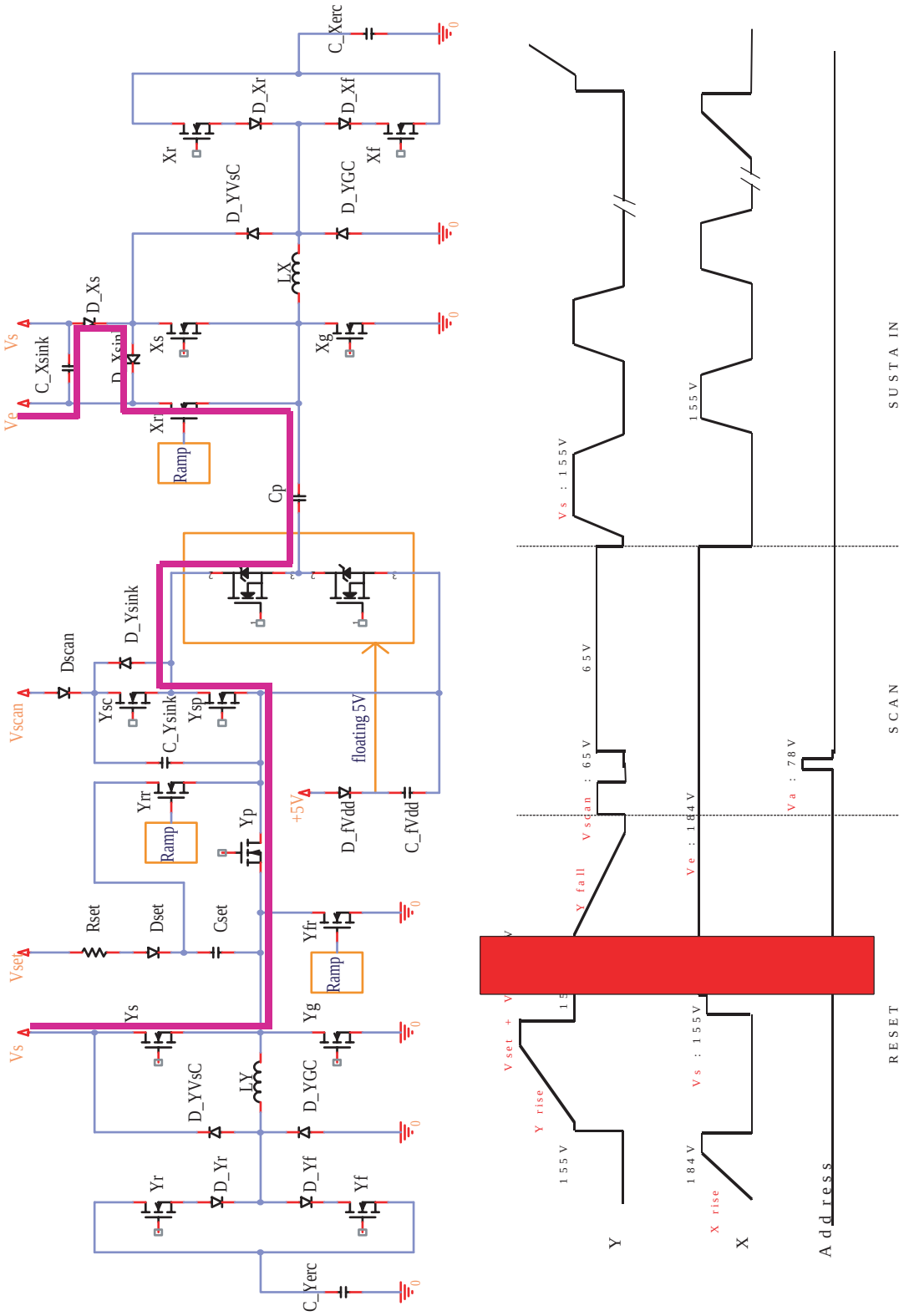
Single scan mode PDP action : Rest section, X : 0 , Y : Vs -> Vs + Vset



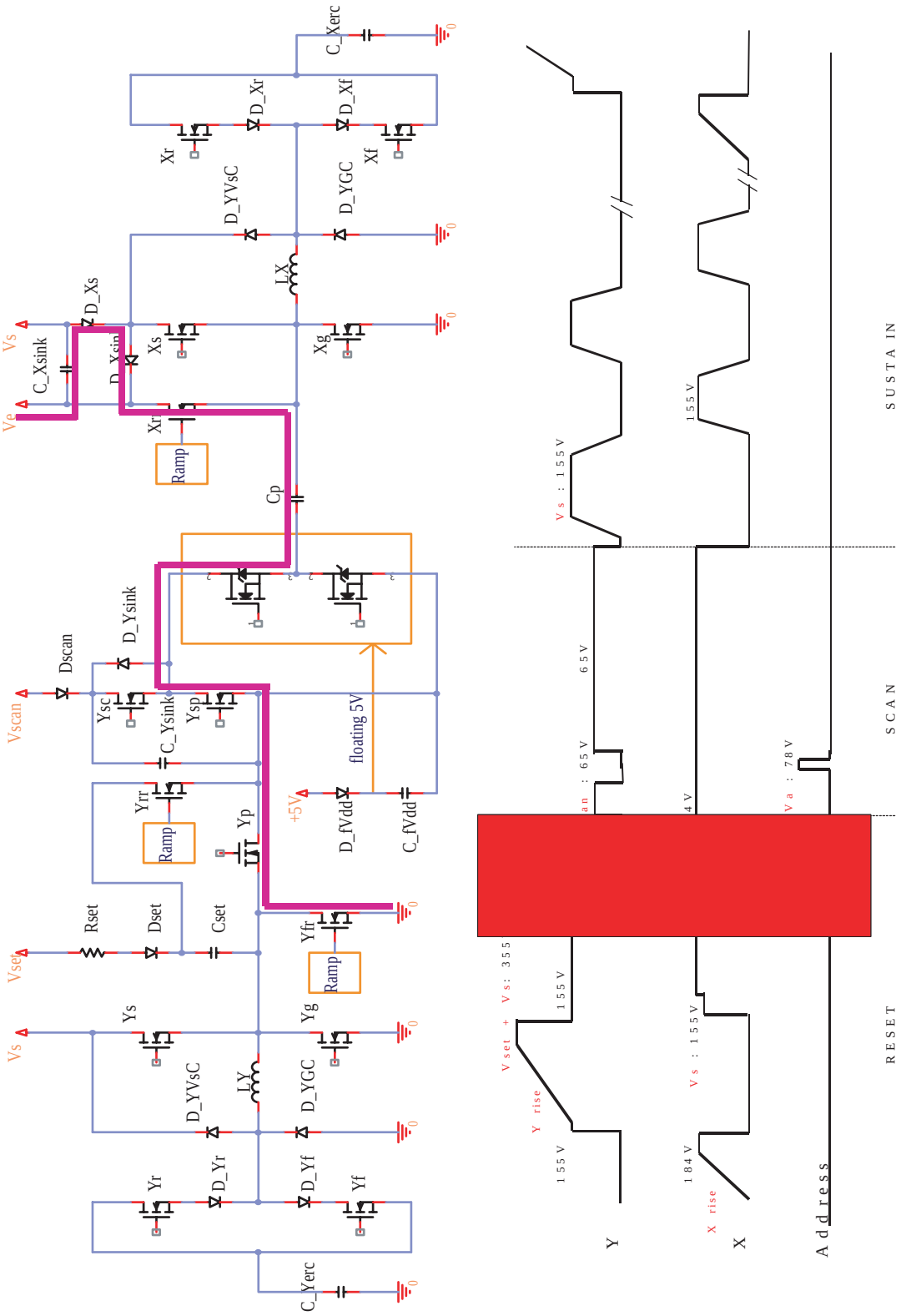
Single scan mode PDP action : Rest section, X : Vs, Y : Vs



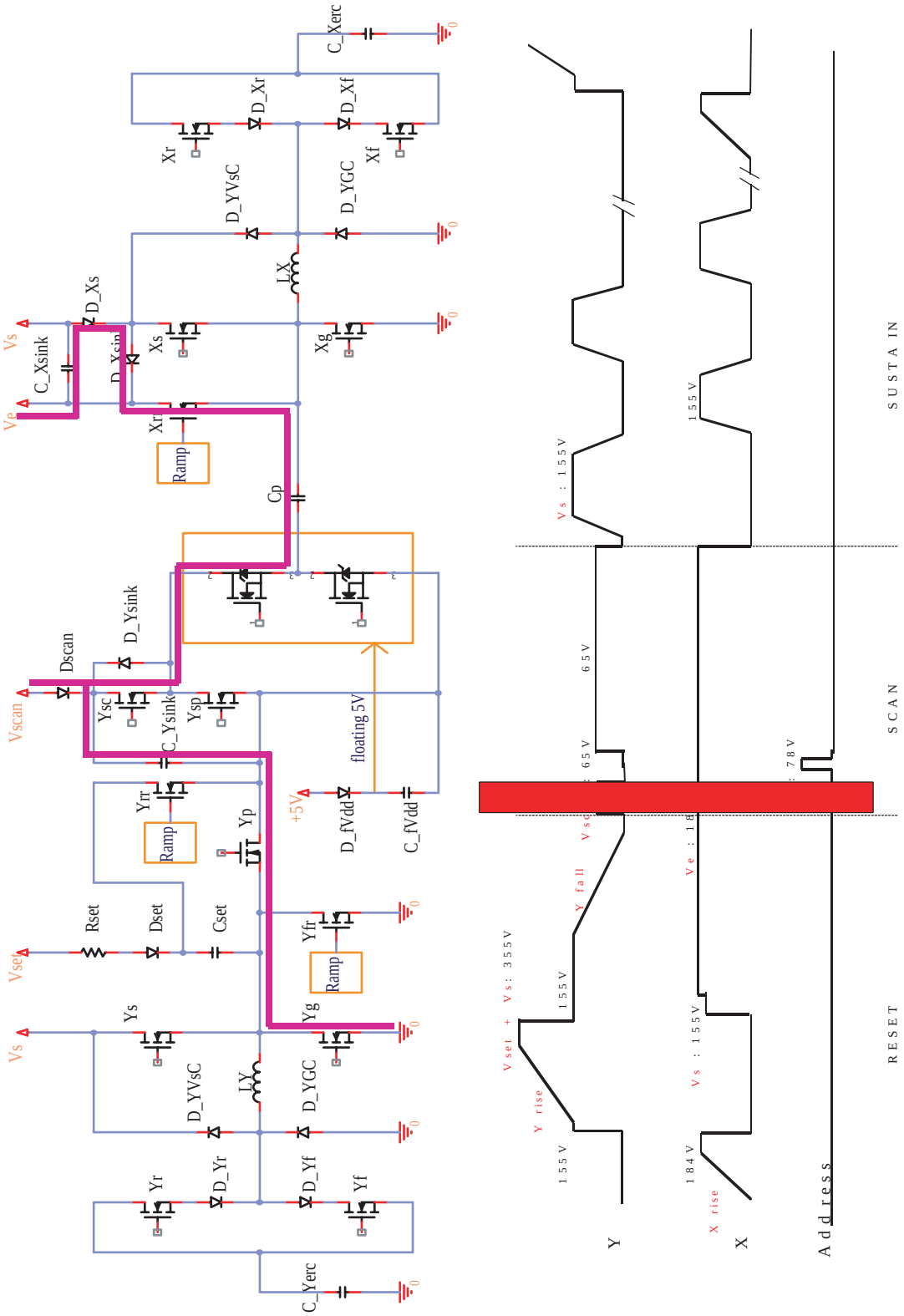
Single scan mode PDP action : Rest section, X : Ve, Y : Vs



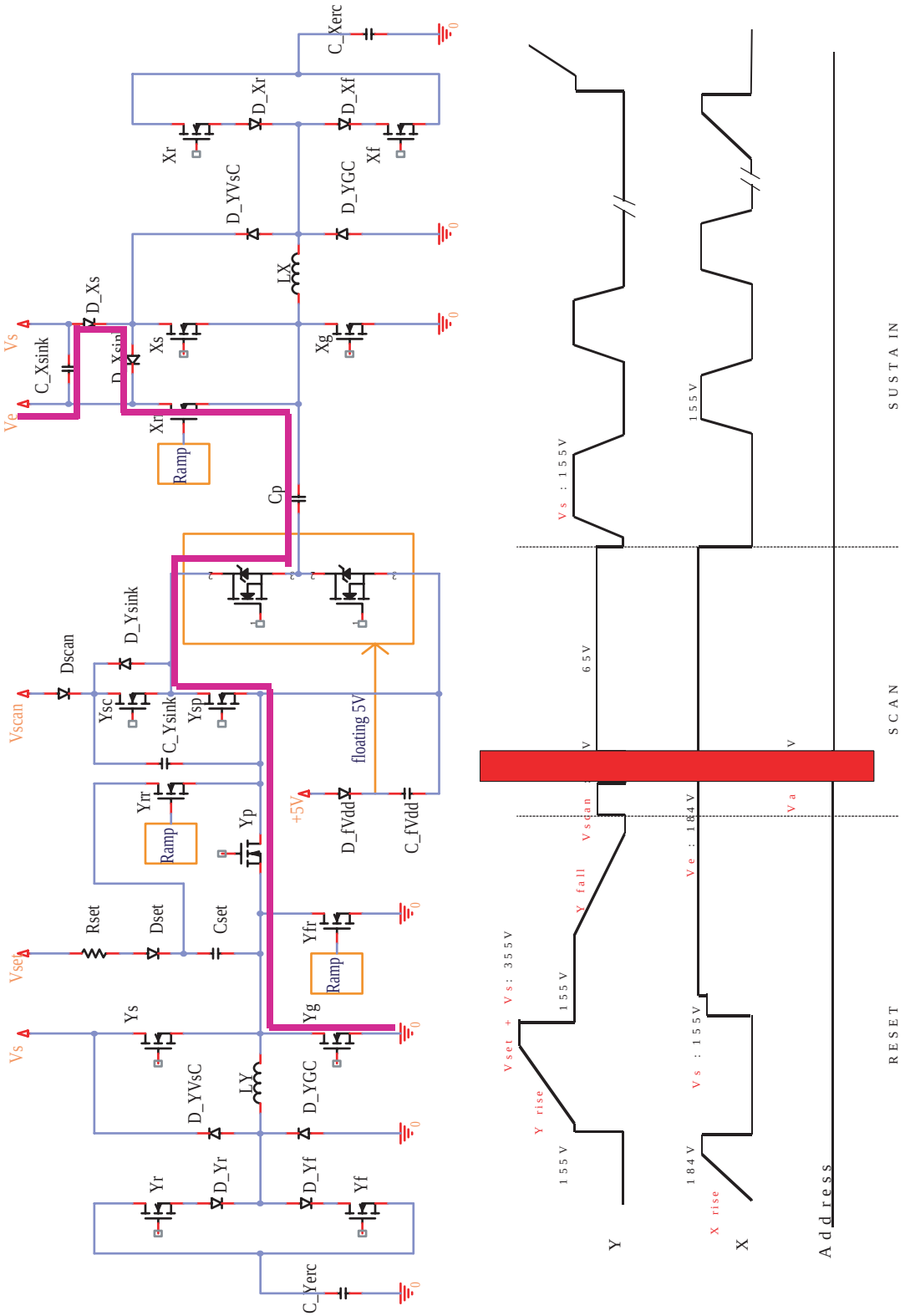
Single scan mode PDP action : Rest section, X : Ve, Y : Vs -> 0



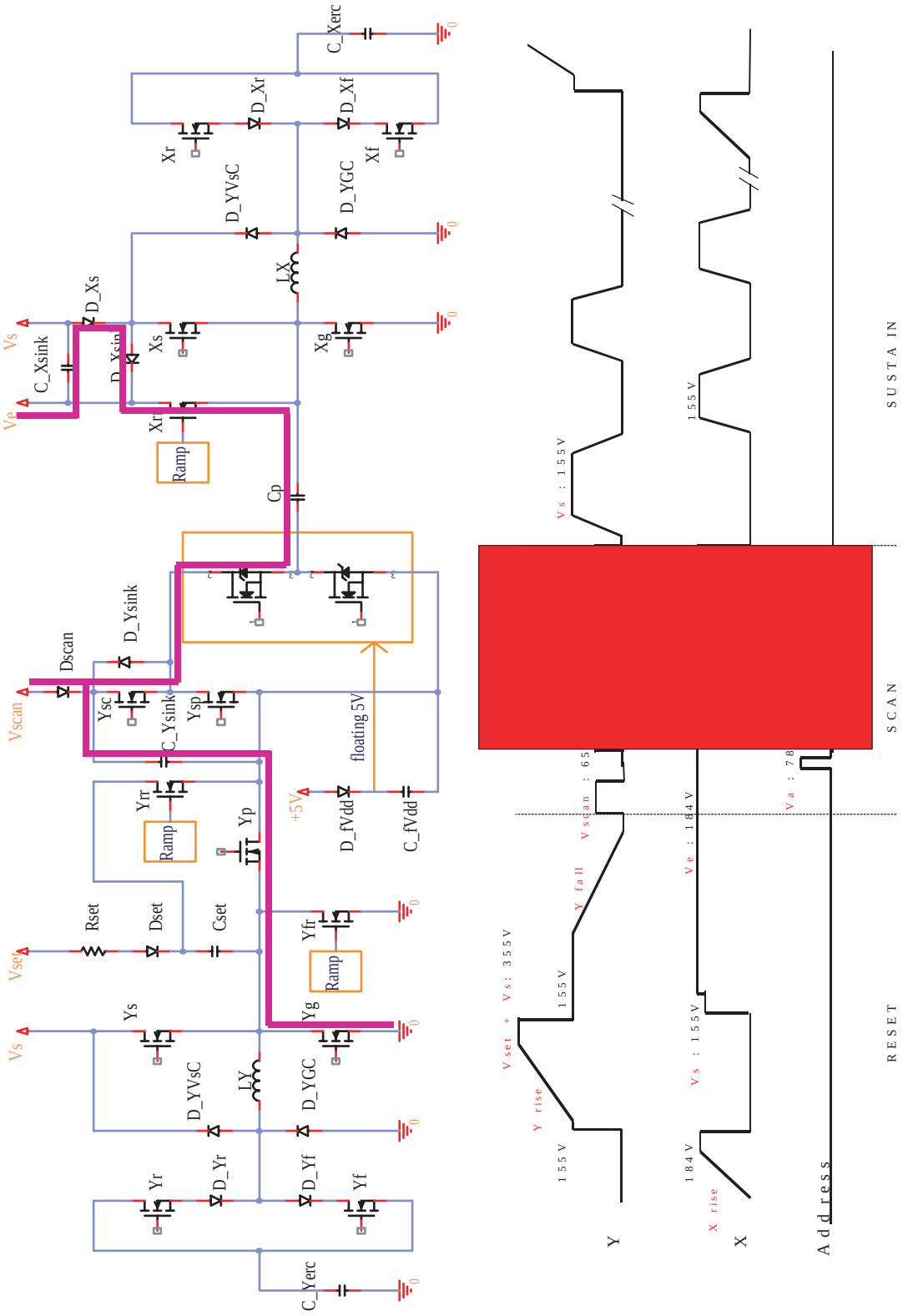
Single scan mode PDP action : Rest section, X : Ve, Y : Vscan, idle scan-line



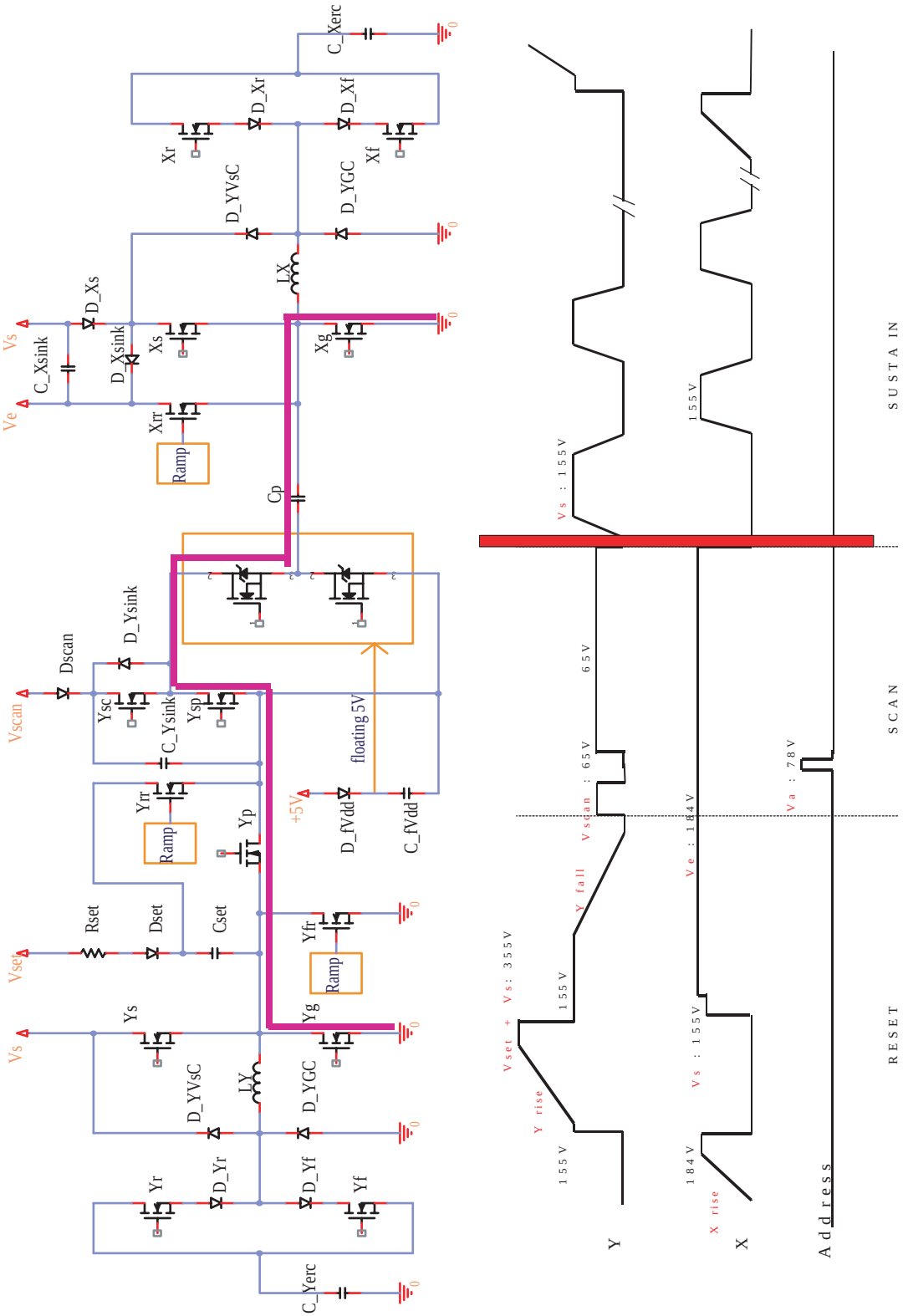
Single scan mode PDP action : Rest section, X : Ve, Y : Vscan, address scan-line



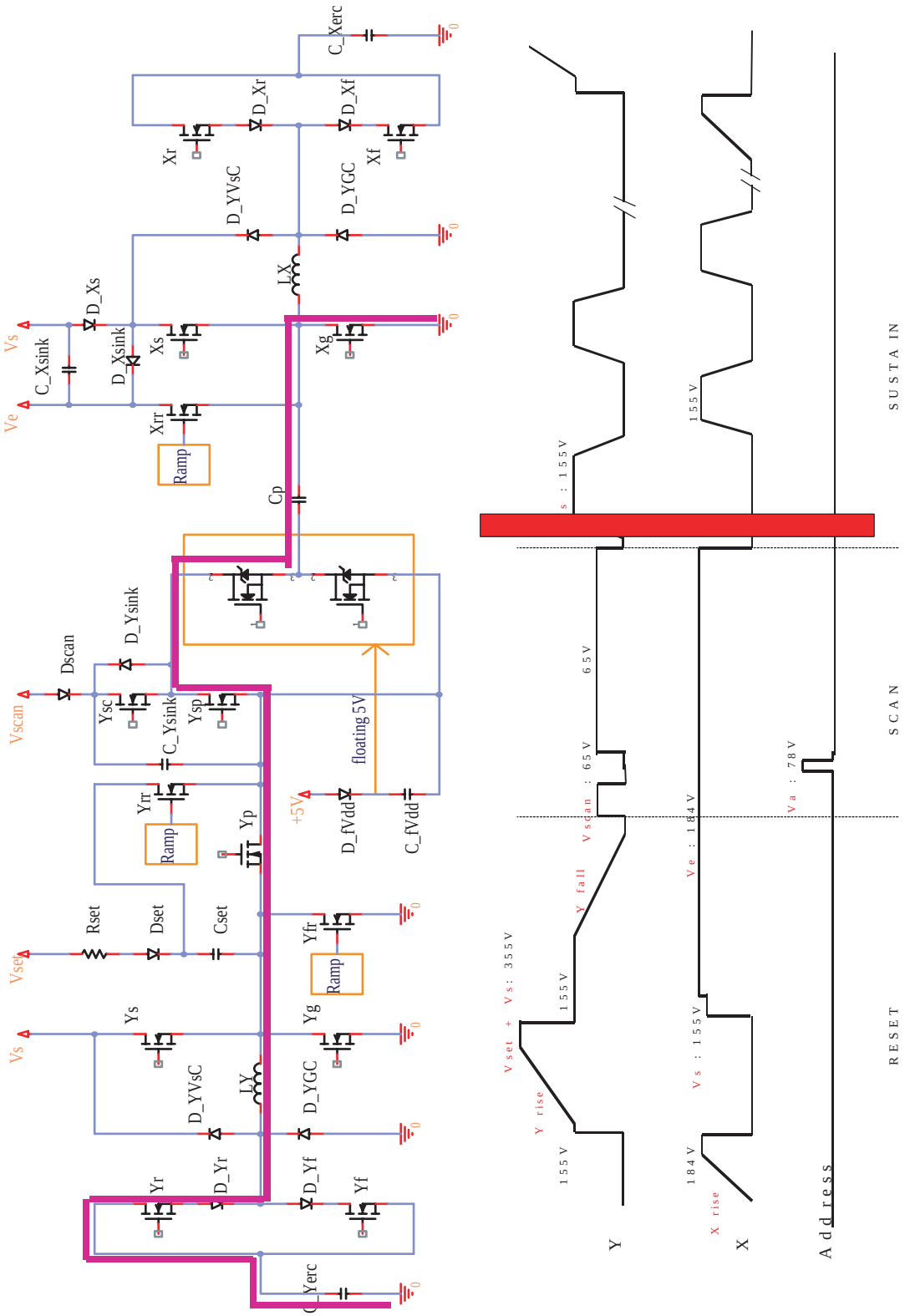
Single scan mode PDP action : Rest section, X : Ve, Y : Vscan, idle scan-line



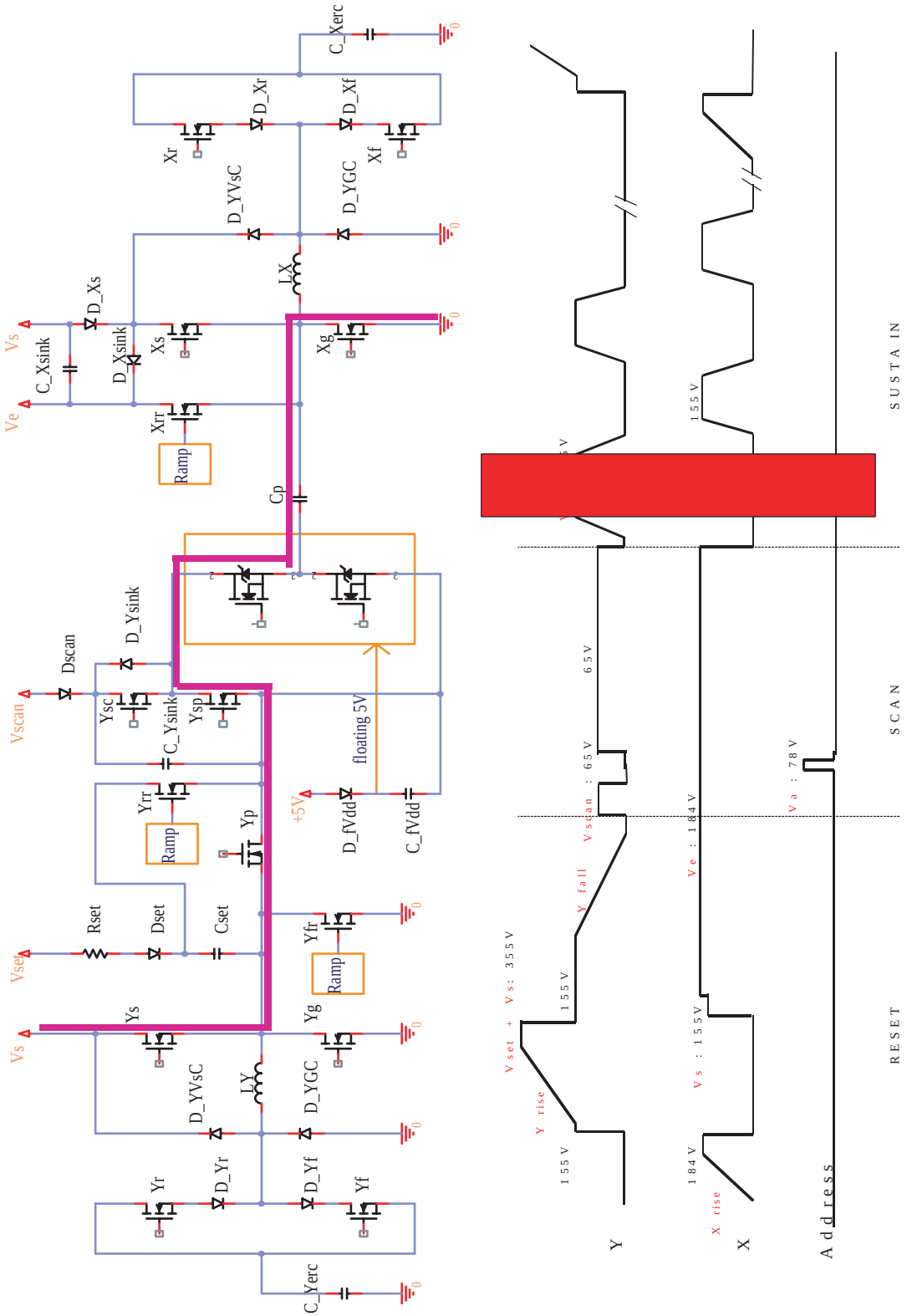
Single scan mode PDP action : Rest section, X : 0, Y : 0, GND mode



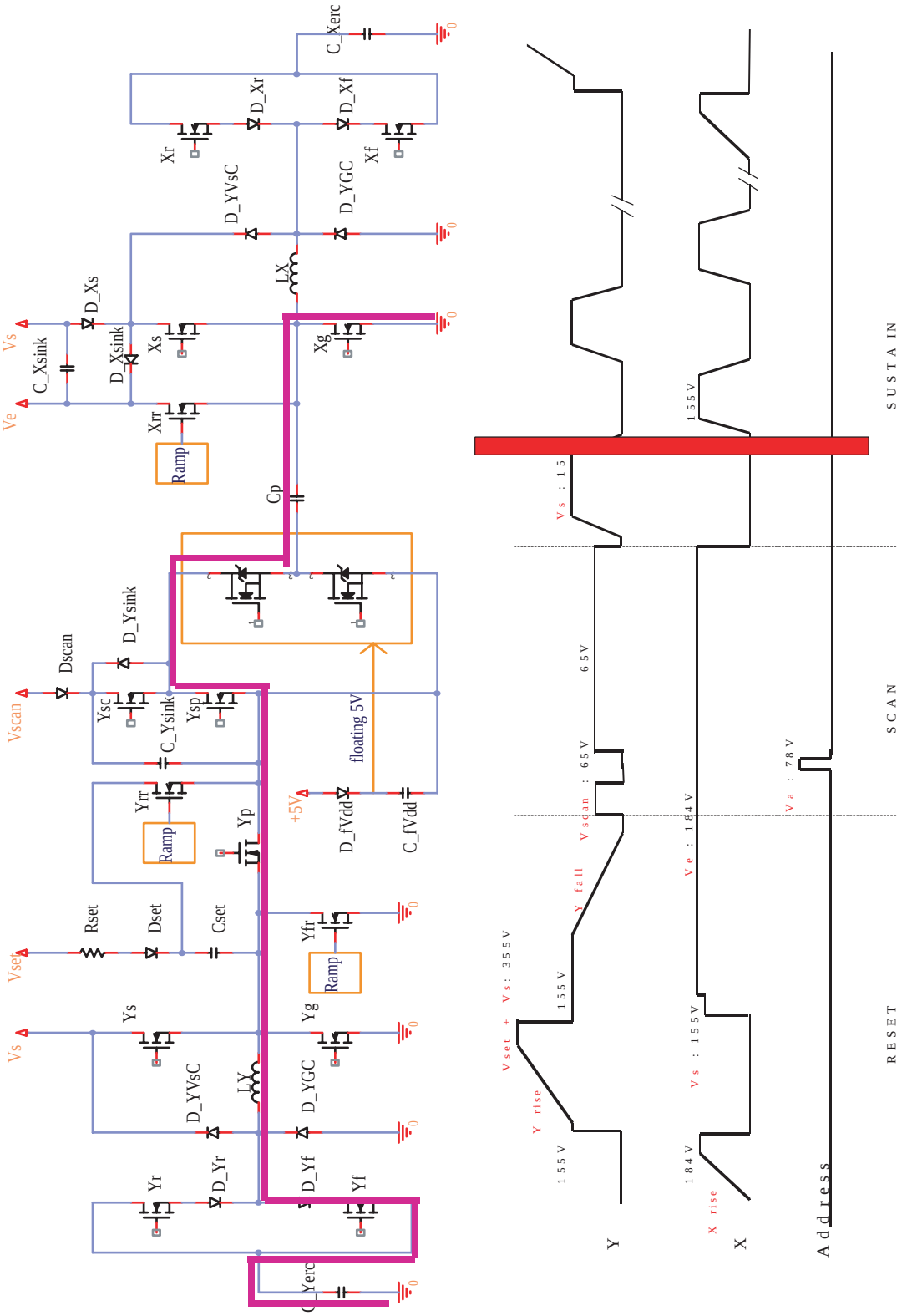
Single scan mode PDP action : Rest section, X : 0, Y : 0 -> Vs, charging mode



Single scan mode PDP action : Rest section, X : 0, Y : Vs, Gas discharging mode



Single scan mode PDP action : Rest section, X : 0, Y : Vs -> 0, discharge mode



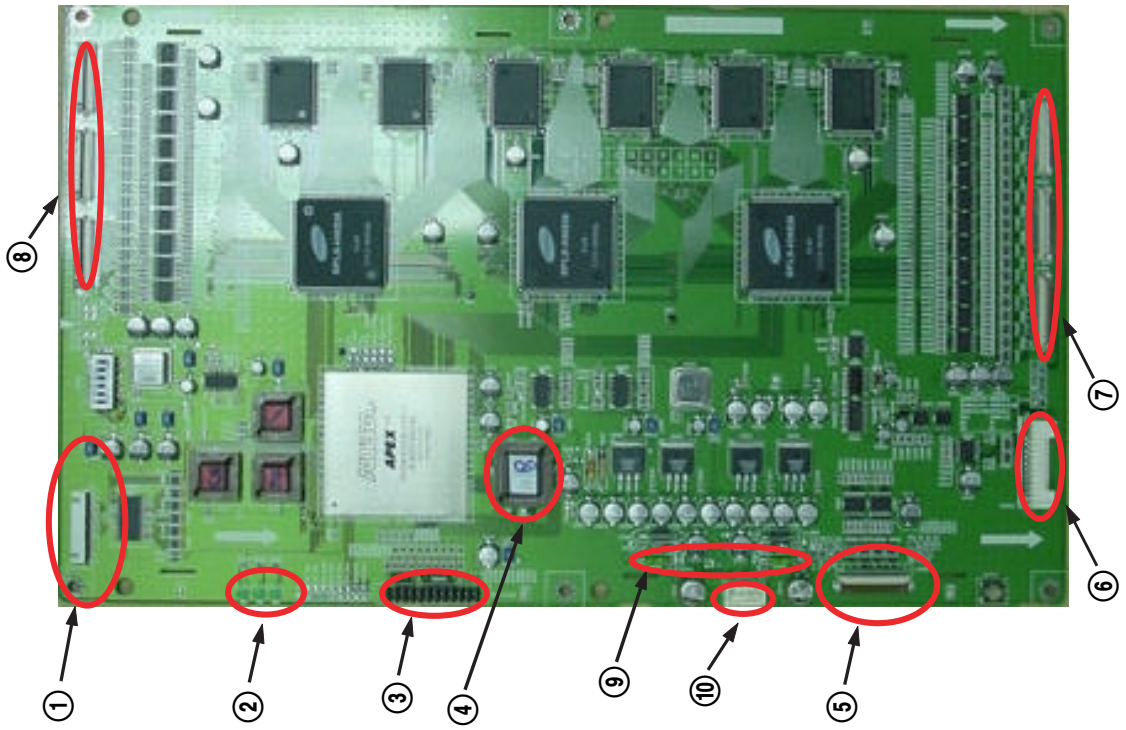
6-3 Logic part

6-3-1 Description of Logic Board

The logic board consists of a logic main board and a buffer board. The logic main board is made up of a data signal processor that processes video signals, and a XY signal generator that runs the XY drivers. The buffer boar stores address driver output sigals and sends them to the address driver IC (COF module).

Logic Board		Function	Remarks
(Logic Main)		- Processes video signals. (W/L, Error diffusion, APC) - Outputs address driver control signals and data signals to the buffer board. - Outputs XY driver board control signals	
(Buffer Board)	E, F, G Buffer oard	Sends data signals and control signalss to the upper COF.	
	H, I, J Buffer board	Sends data signals and control signals to the lower COP.	

6-3-2 Name and Description of Major COmponents of the Logic Board



NO	NAME	Description
① C	LVDS Connector	An input connector that receives LVDS encoded RGB, H, V, DATAEN, and DCLK signals from the video board.
② (	Operation LED	Indicates if the logic board properly receives Sync and clock signal.
③	Key Scan Connector	A connector to the Key Scan board that check and adjust 24C16 data.
④	256K	An EEPROM for saving the gamma table, the APC table, the drive signal timing and other options, etc.
⑤	Y Connector	A connector that outputs Y driver board control signals.
⑥	X Connector	A connector that outputs X driver board control signals.
⑦	Address Buffer Connector (E,F,G)	A connector that outputs address data and control signals to the E,F and G buffer board.
⑧	Address Buffer Connector (H,I,J)	A connector that outputs address data and control signals to the H,I and J buffer board.
⑨	Power Fuse	A fuse connected to the power source (5V) of the logic board.
⑩	Power Connector	A connector that supplies power (5V) to the logic board.

6-3-3 Waveform in Normal Operation

If the PDP unit and the logic board are operationg properly, the LED LD2010 in Figure 1 will blink at about a 1 second interval.
If the unit is out of order, check the status of the Operation LED through eye-inspection first.
If the behavior of the Operation LED is different from that of normal operation, you have to replace the board. To trouble-shoot the board, complete the logic board test procedures attached in the Appendix.

6-3-3(A) Layout and Apperance of the Board

(1) Input

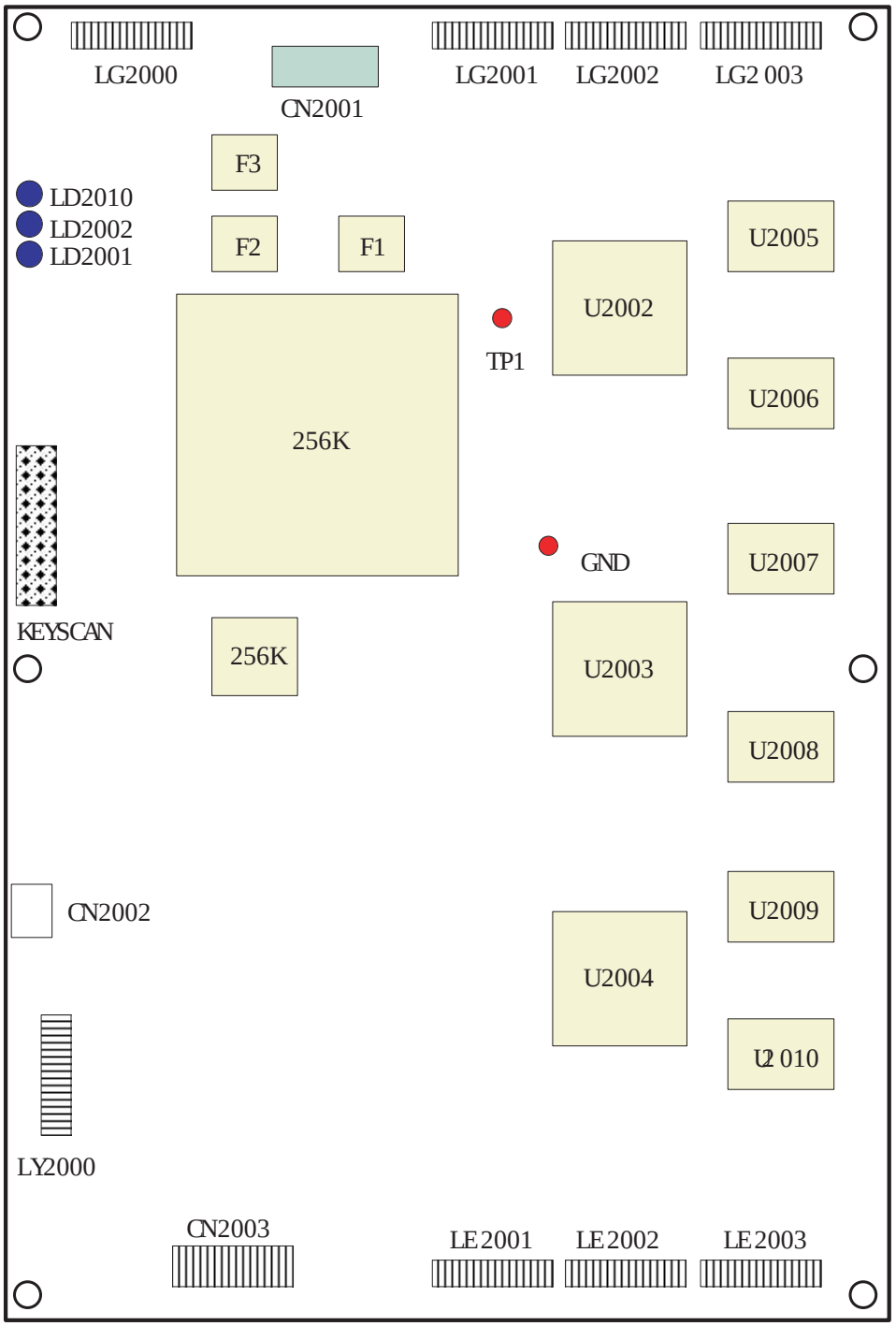


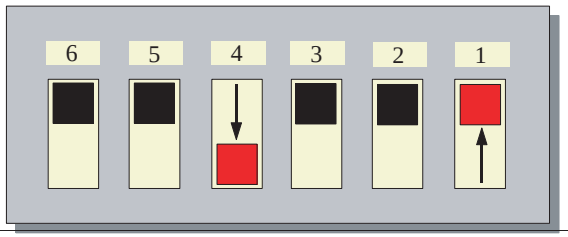
Fig. 1 Layout of the Logic Mainboard

(2) Appearance of and Markings on the Connector

Basically, it is depicted exactly the same as the real one on the PCB.

6-3-3(B) DIP Switch setting that selects the internal or external clock (CN2001)

(1) External Mode Selection

MODE	PAGE	REGISTER ADDRESS	EXTERNAL MODE VALUE	DIP SWITCH STATE EXTERNAL MODE
NTSC	00	2E	01	

☞ When External Mode is selected;

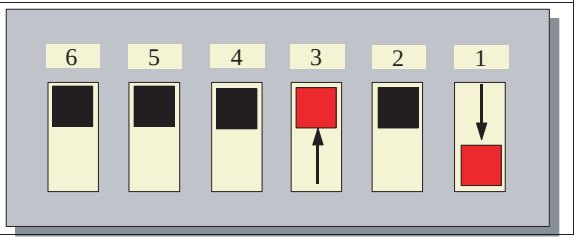
① Enter PAGE 00.

② Set Register 2E's address to 01.

③ Adjust the Dip Switch as shown above.

(UP : PIN_NUMBER 6,5,3,2,1 / DOWN : PIN_NUMBER 4)

(2) Internal Mode NTSC Pattern Selection

MODE	PAGE	REGISTER ADDRESS	INTERNAL MODE VALUE	DIP SWITCH STATE INTERNAL MODE
NTSC	00	2E	00	

☞ When Internal Mode Pattern is selected;

① Enter PAGE 00.

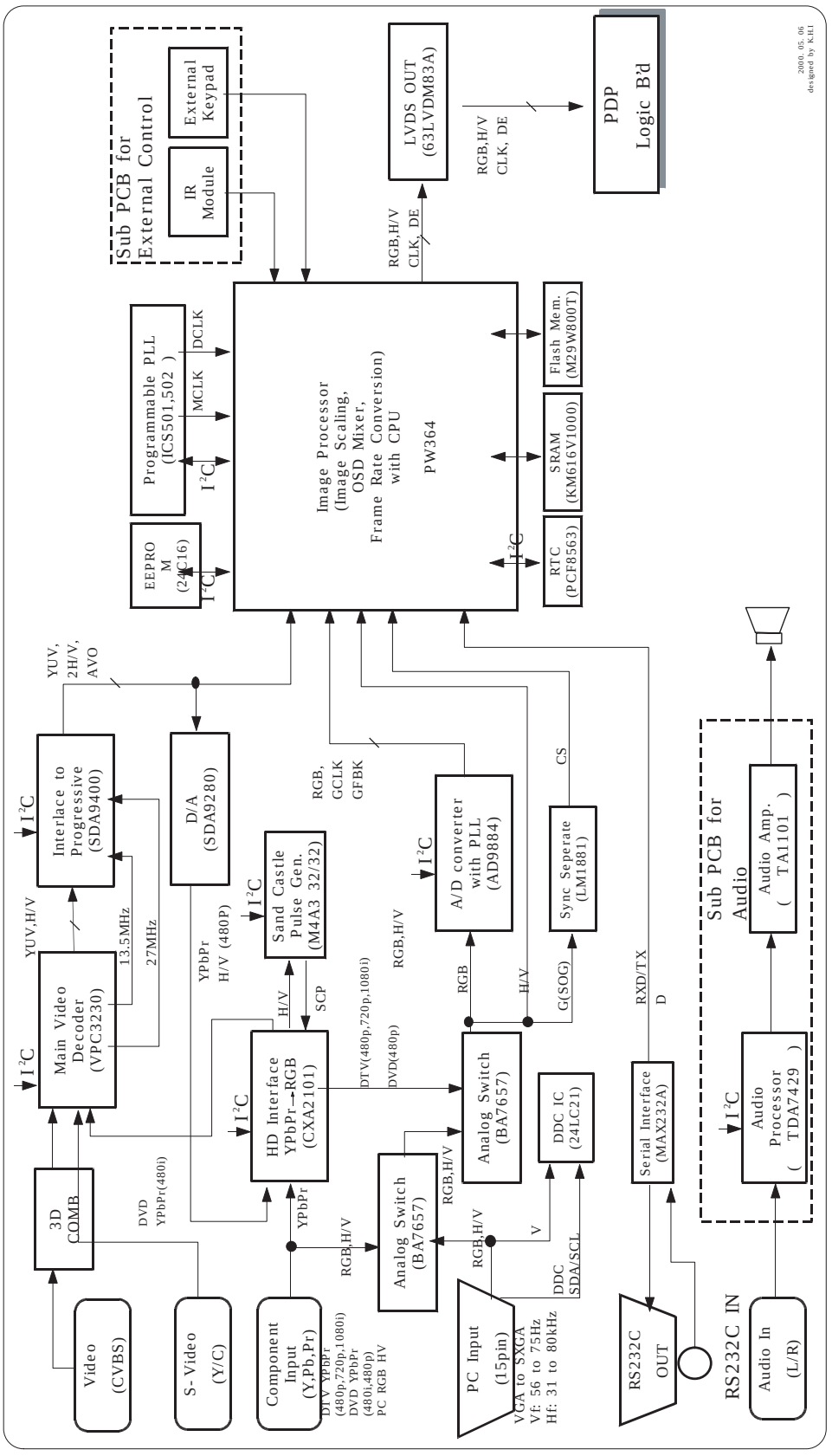
② Set Register 2E's address to 01.

③ Adjust the Dip Switch as shown above.

(UP : PIN_NUMBER 6,5,4,3,2 / DOWN : PIN_NUMBER 1)

6-4 Scaler Board Block Diagram & Description

6-4-1 General Signal Process B/D



6-4-2 Description in Signal Process Block

► 3D COMB FILTER : This 3D Comb Filter is used to improve noise and picture quality by three-dimensionally adjusting the signal from the Input Video jack. The input signal is received from CVBS and the picture is digitally improved via A/D Conversion and FIELD MEMORY. And then the signal is output as the ANALOG YC signal.

► VPC3230 : This functions as a video decoder, which can receive all of the YC, YUV, CVBS inputs.
In addition, this converts Y/C into YUV after receiving 3D Comb Output Y/C, S-Vido Y/C, and DVD YUV.

► VIDEO DOUBLER : Usually, the current video image adopts the INTERLACE Scanning system and it has poor video because of Flicking on the screen. Using the SDA9400 , INTERLACE is converted into PROGRESSIVE in order to improve the quality of video.

► VIDEO PROCESSOR : Since the HD modes like 1920*1080I have higher video bandwidth than the existing video signals, the ordinary decoder like VPC3230 can't handle those modes. PC has higher bandwidth of video signal than TV and the RGB video format.
Therefore, if the HD signal can be converted into the RGB signals, the TV video signal can have the same processing as the PC VIDEO signal. CXA2101 developed by SONY is used to convert YPbPr into RGB.
CXA2101 converts both DTV signals and all the SD signals processed in the sequence of SDA9400 then SDA9280 into RGB.
This processor performs some user control functions, such as tint, color, and sharpness.
Also, it controls high light gains low light offsets when doing white balance adjustments.

► ANALOG SWITCH : The video decoder like VPC3230 has a built-in video switch that assigns one signal out of various received inputs, though most of ICs for PC are designed so that they support only one source because of less necessity of simultaneously processing the multi inputs. To process the input source of MULTI (PC&HD), therefore, a function of selecting an input should be externally added; as is performed by ROHM's BA7657F. PW364 transmits a signal determining which input is selected.

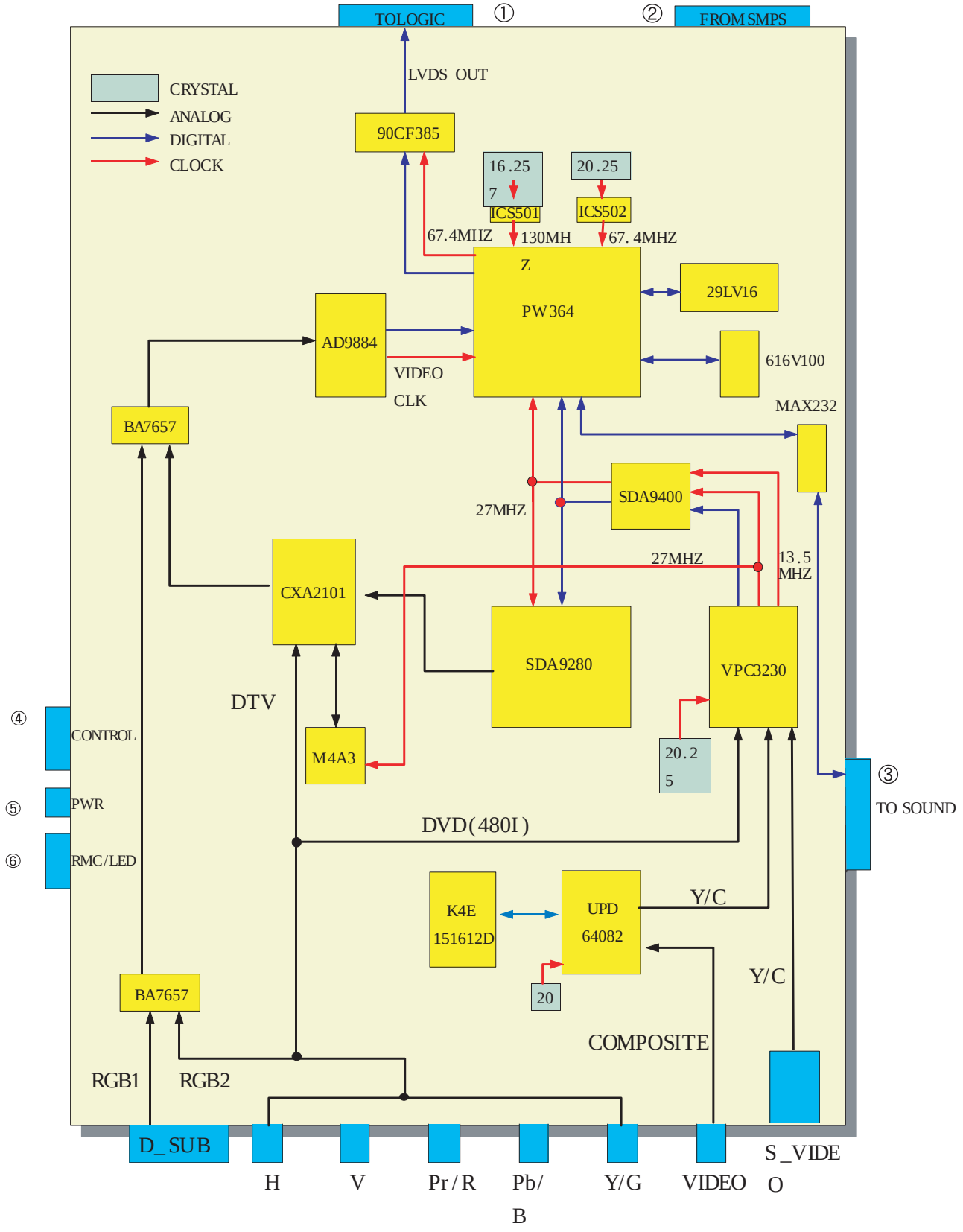
► ADC : A device that converts the input RGB signals into the 8bit DIGITAL RGB signals.
In case of white balance adjustments, this device sets the color temperature by controlling R/B gains and R/B offsets.

► PW364 : PW364 is a multi-functional scaler which one chip has video signal scaling, 8086 CPU, 4M BYTE VIDEO MEMORY functions. The PC and Video input signals are received from GRAPHIC PORT and VIDEO PORT, respectively.Its main functions include UP/DOWN SCALING, PIP, ZOOM, GAMMA CORRECTION, Compensation of GEOMETRIC DISTORTION, powerful GRAPHIC OSD.

► FIRMWARE : Mounted is a software that is used for system control by operating 8086 built in PW364. A 4MBIT FLASH ROM is mainly used, but one up to 8MBIT can be used according to PROGRAM and capacity of OSD DATA. The system is easy to maintain because programming can be re-done at any yime using the FLASH ROM.

6-5 IC Line-Up

6-5-1 IC LINE UP

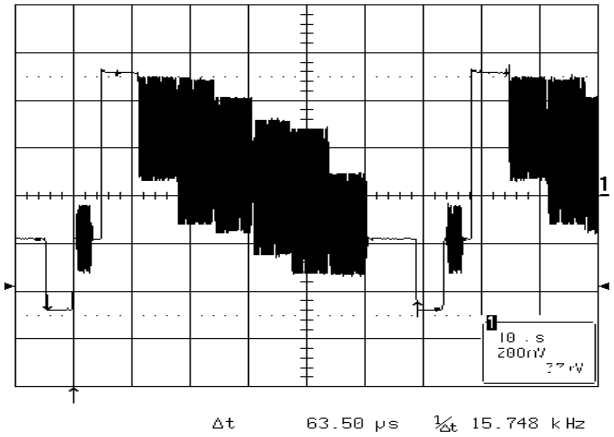


6-5-2 PIN Description

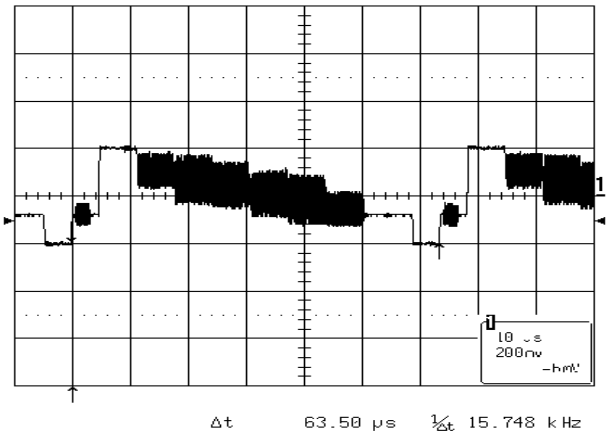
	①	②	③	④	⑤	⑥
Pin No.	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name	Pin Name
1	DGND	ST5V	SDA	GND	KEY4	ST5V
2	DGND	GND	SCL	KEY1	GND	GND
3	TxOUT0-/RxIN0	GND		KEY1	KEY4	RMC SIG
4	TxOUT0+/RxIN0	D5V	T1	KEY1		LED R
5	DGND	REL_SW	R1	KEY4		LED G
6	DGND	TEMP DET	T2	GND		
7	TxOUT1-/RxIN1	FAN DET	R2			
8	TxOUT1+/RxIN1	GND	GND			
9	DGND	GND	AMP MUTE1			
10	DGND	12V	GND			
11	TxOUT1-/RxIN1	12V				
12	TxOUT1+/RxIN1	A6V				
13	DGND	GND				
14	DGND					
15	TxCLKOUT-/RxCLKIN-					
16	TxCLKOUT-/RxCLKIN					
17	DGND					
18	DGND					
19	TxOUT3-/RxIN3-					
20	TxOUT3+/RxIN3+					
21	NC					
22	NC					
23	NC					
24	NC					
25	NC					
26	NC					
27	NC					
28	NC					
29	NC					
30	NC					
31	NC					

6-6 Main I/O signal pules and voltages

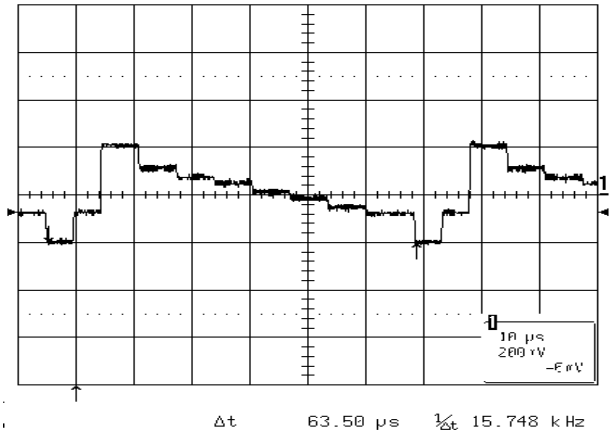
6-6-1 Signal Pulses of Image Board(Input Signal Conditions : 7 Color bar)



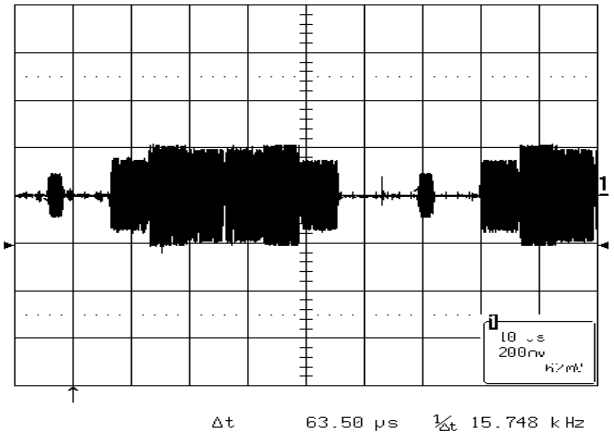
* 9C55 VIDEO INPUT



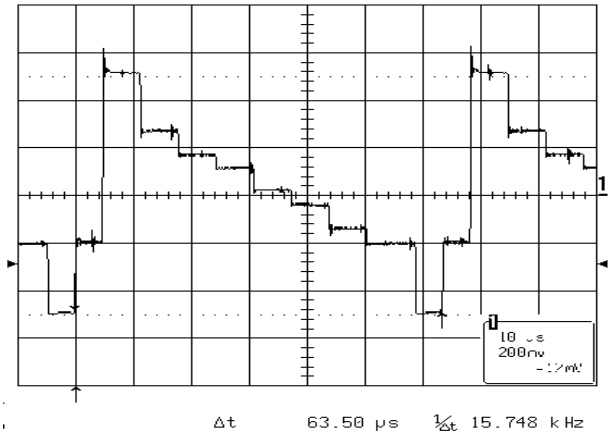
*3D COMB P88 VIDEO INPUT



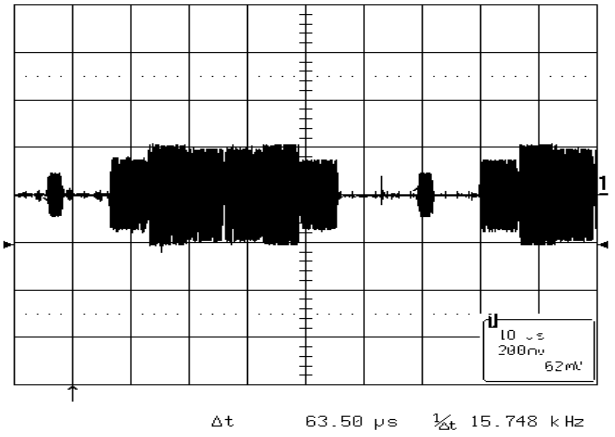
* 3D COMB P84 Y OUTPUT



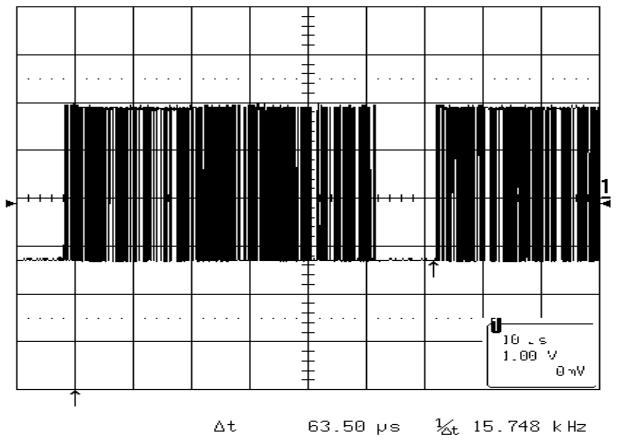
*3D COMB P83 C OUTPUT



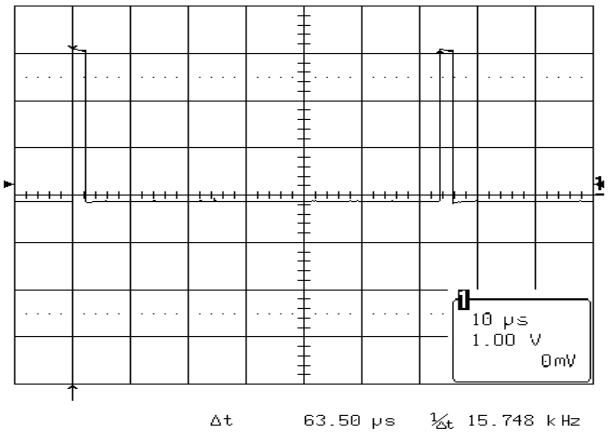
* 3U1(VPC3230) PIN75 Y_IN



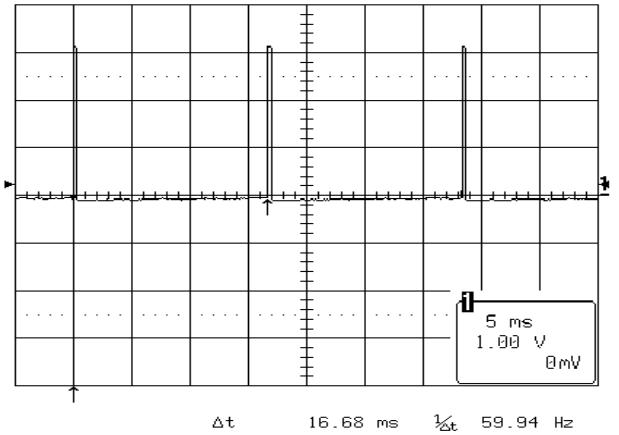
* 3U1(VPC3230) PIN72 C_IN



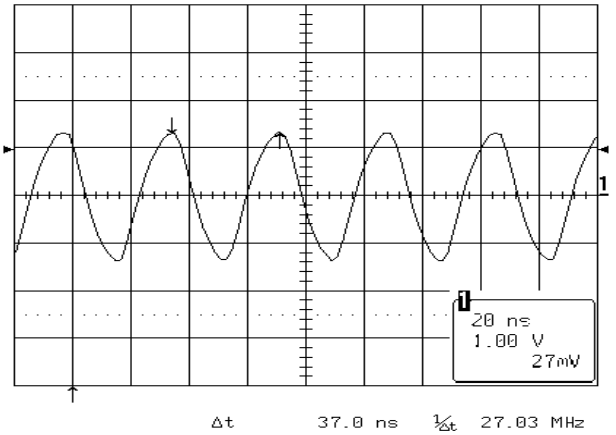
* 3U1(VPC3230) PIN40 Yo_OUT



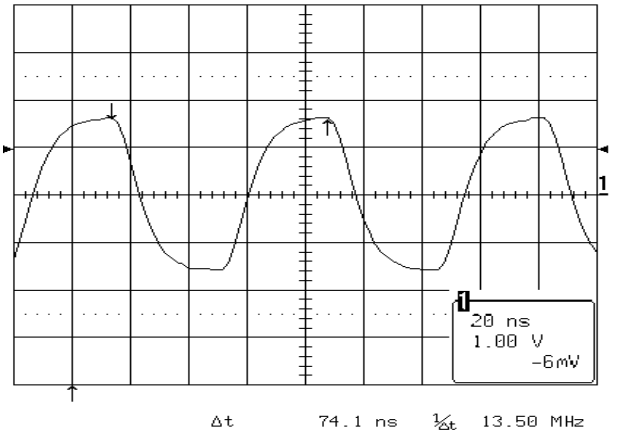
* 3U1U(VPC3230) PIN56 HS_OUT



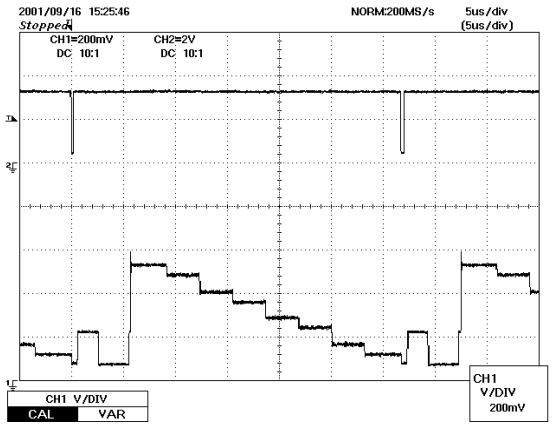
* 3U1(VPC3230) PIN57 VS_OUT



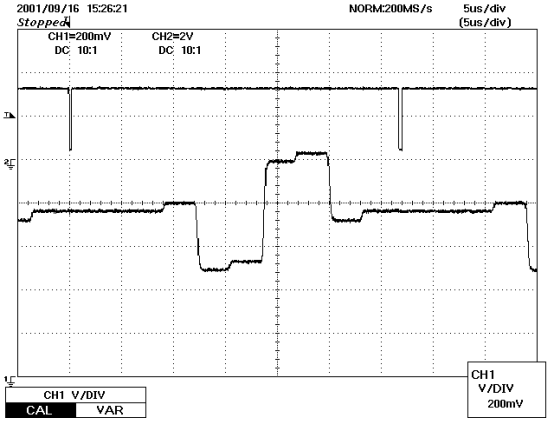
* 3U1(VPC3230) PIN27 LLC2_OUT



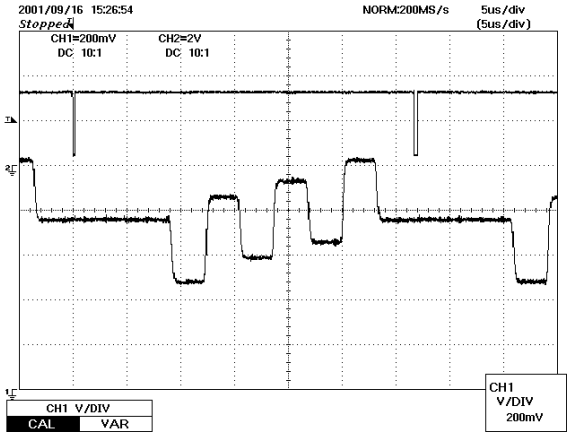
* 3U1(VPC3230) PIN28 LLC1_OUT



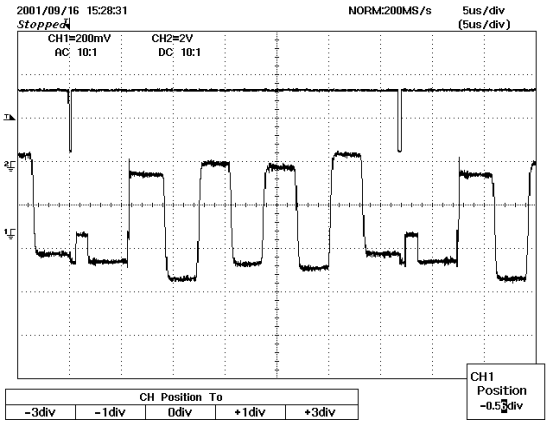
* 3U2(SDA9280) PIN47 V_Y_OUT



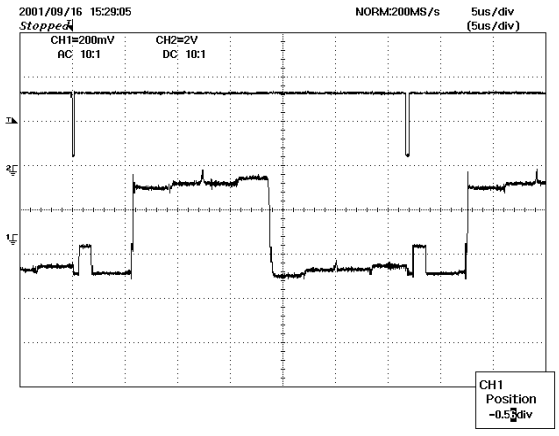
* 3U2(SDA9280) PIN51 V_Pr_OUT



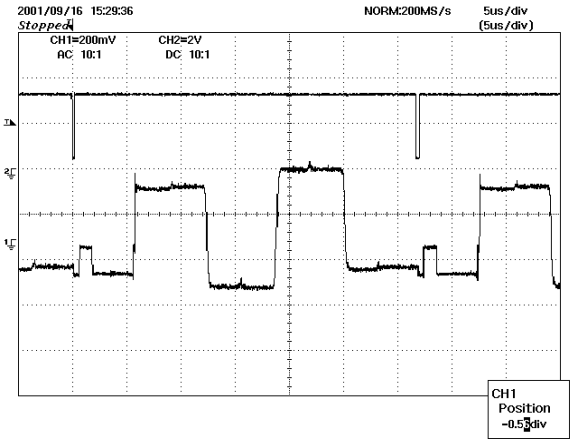
* 3U2(SDA9280) PIN54 V_Pb_OUT



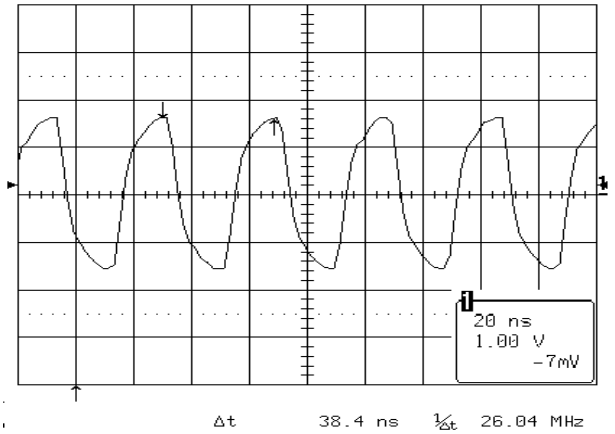
* 2U2(CXA2101) PIN39 B_OUT



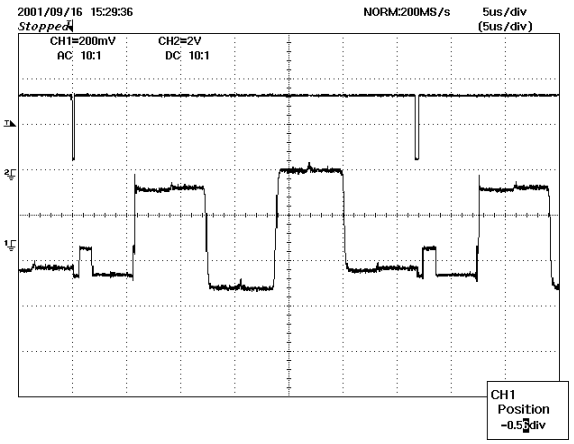
* 2U2(CXA2101) PIN37 G_OUT



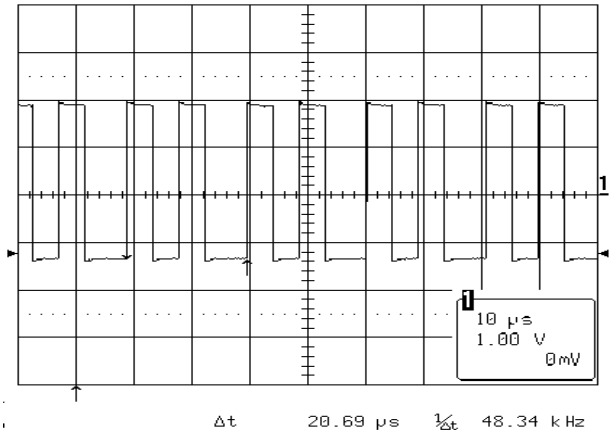
* 2U2(CXA2101) PIN35 R_OUT



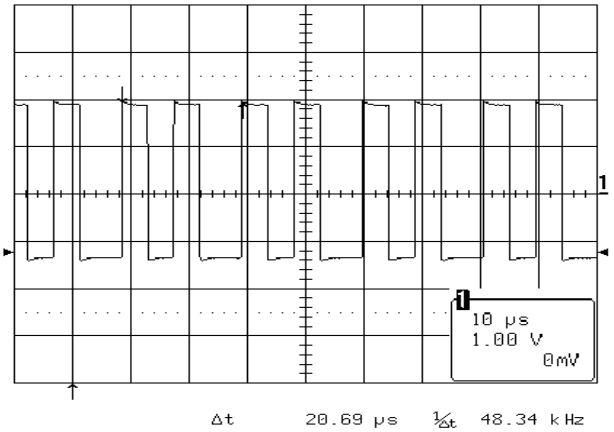
* 1U1(AD9884) PIN:115 PCLK_OUT



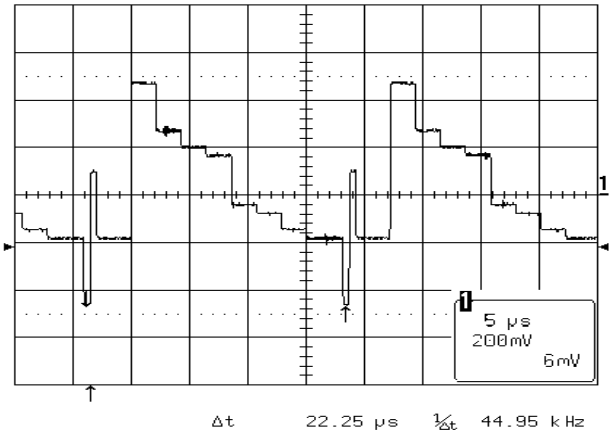
* U29(AD9884) PIN7 R_IN



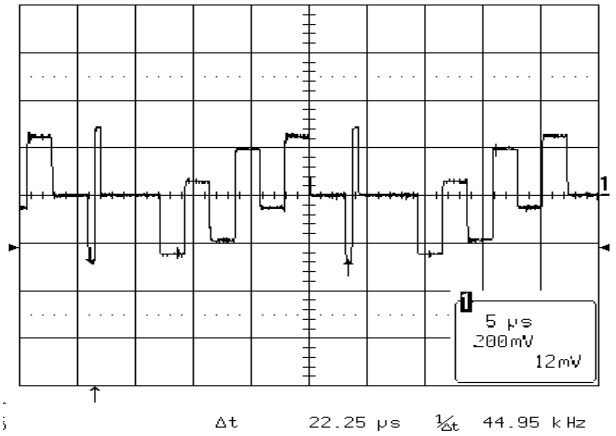
* U29(AD9884) PIN95 ROUT_ODD



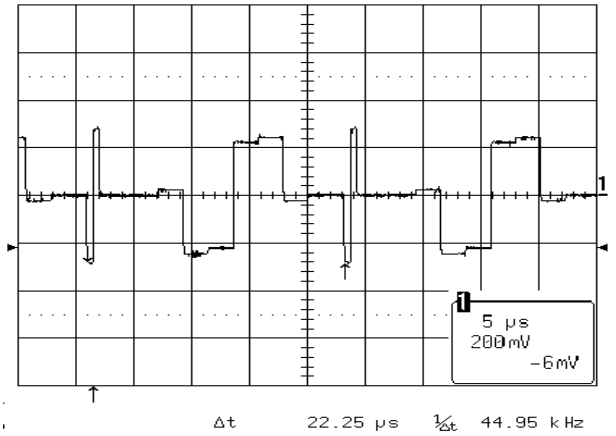
* U29(AD9884) PIN105 ROUT_EVEN



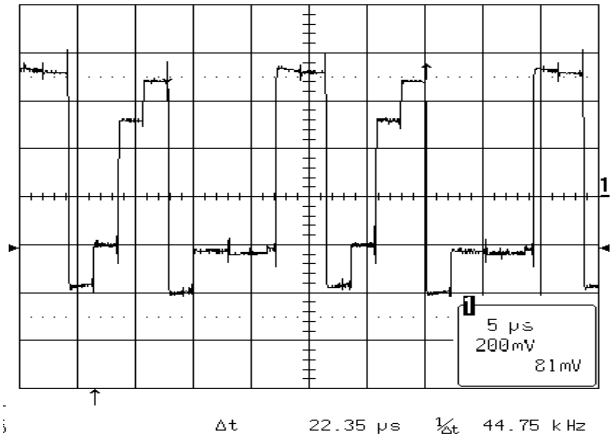
* 2U2(CXA2101AQ) PIN5 DTV.Y_IN



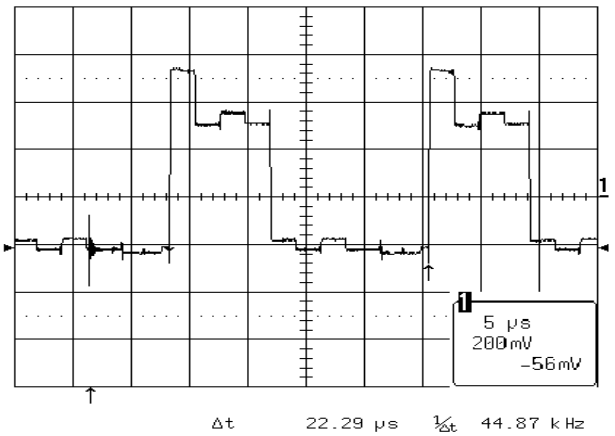
* 2U2(CXA2101AQ) PIN4DTV.Pb_IN



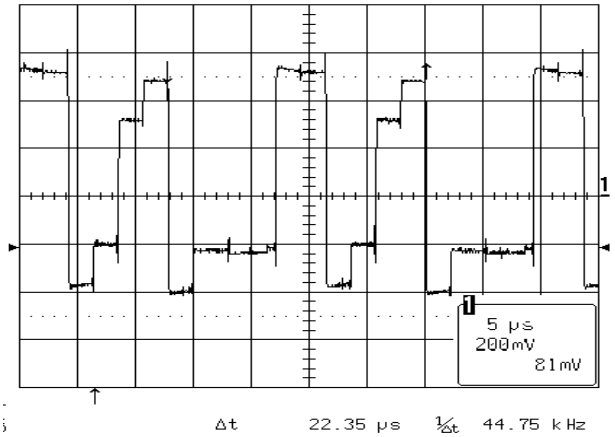
* 2U2(CXA2101AQ) PIN3 DTV.Pr_IN



* 2U2(CXA2101AQ) PIN35 DTV.R_OUT



* 2U2(CXA2101AQ) PIN37 DTV.G_OUT

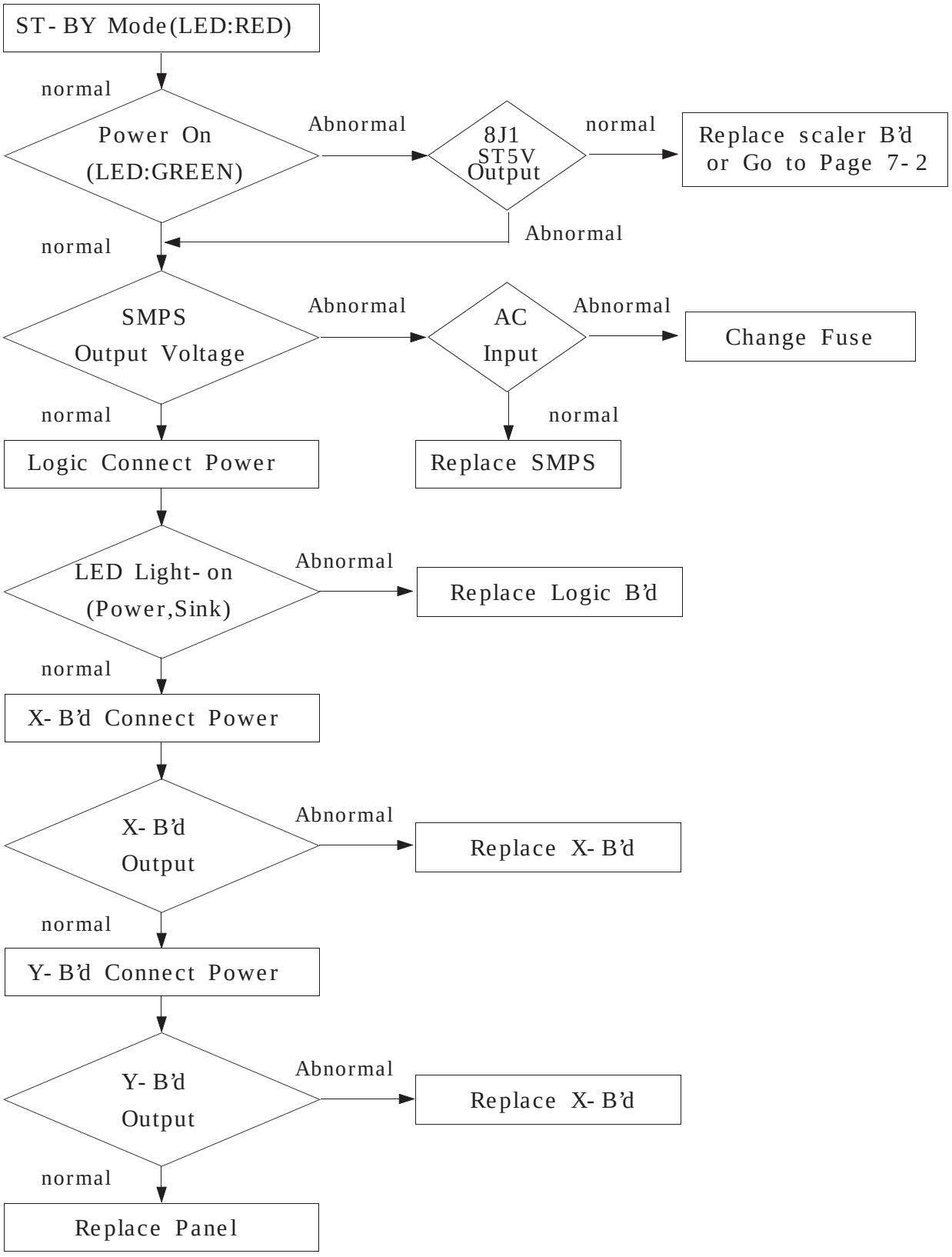


* 2U2(CXA2101AQ) PIN39 DTV.B_OUT a

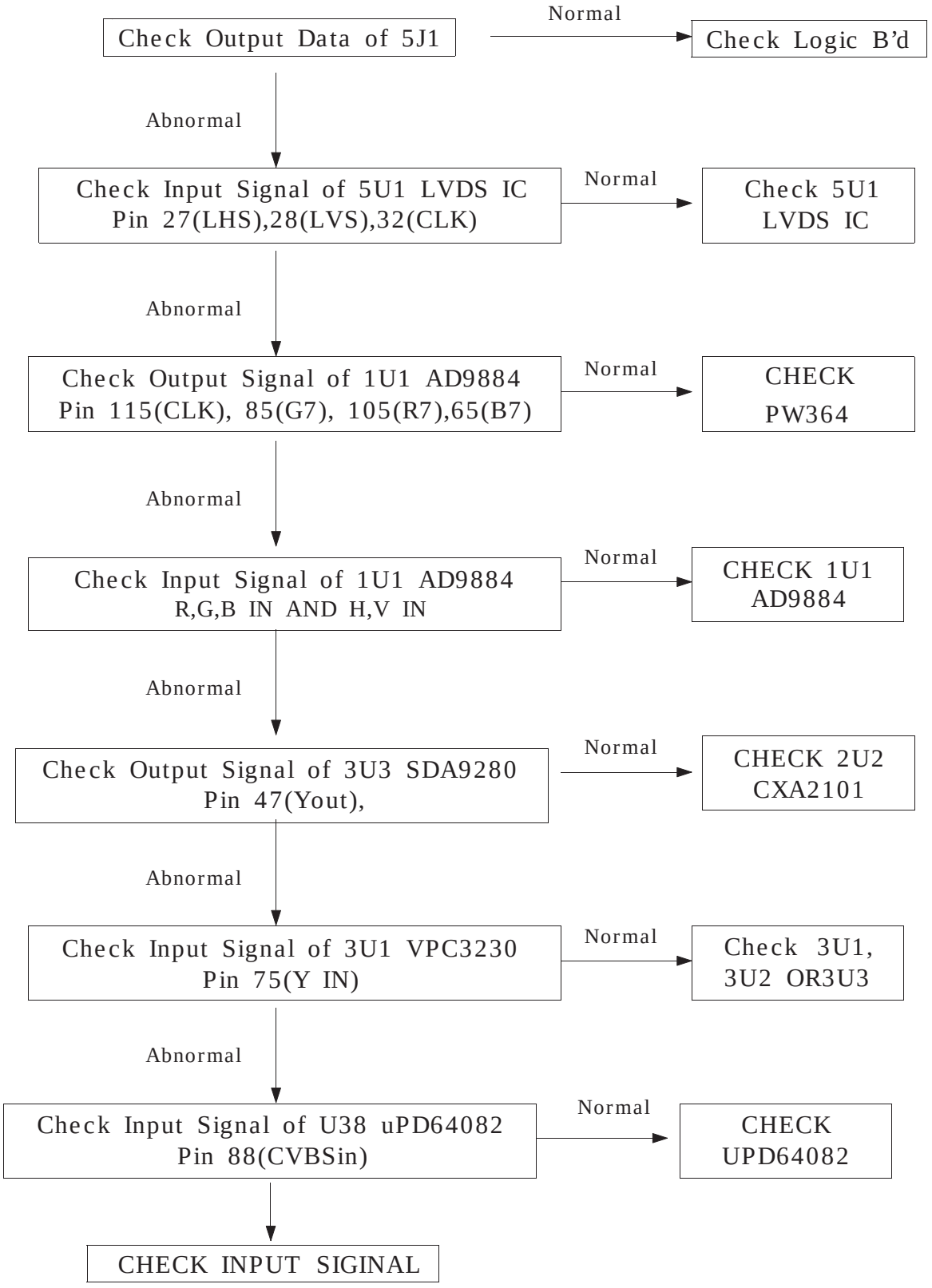
MEMO

7. Troubleshooting

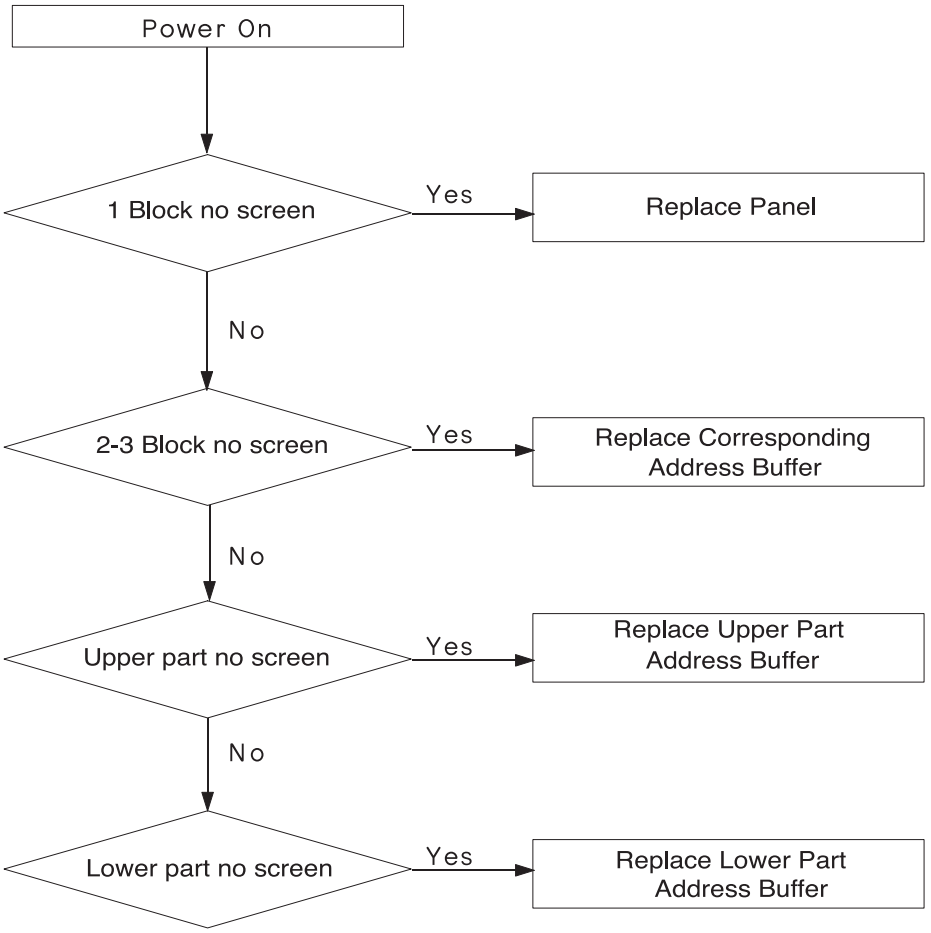
7-1 No Raster(Board Change in PDP Monitor)



7-2 No Raster in Scaler Board



7-3 Partly no screen



7-4 63"HD s1.0 Logic Main Board T/S

If the PDP unit and the logic board operates properly, the operation LED of Figure 1 would blink at about 1 second interval.

If the unit is out of order, check the status of the operation LED through eye-inspection first.

If the behavior of the operation LED is different from that of normal state, you have to replace the board.

To check the trouble on the board, complete the following logic board test procedures described below.

Required testing equipment	:	- Oscilloscope (digital 400 MHz with more than 3 channels)
		- Multi-meter
Other equipment	:	- DC power supply (5V: 1EA)
		- Sub-PCB ASS'Y for JIG: 1 EA

① Perform eye-inspection and short circuit inspection on the power stage of the logic board to be examined. If no problem is found, perform the following examinatios on the board in order.

② Change the clock setting of the logic board to internal.

③ Connect the power (5V) to LD1, and check that the LED (LD2000) on the top left of the board blinks at about a 1 second interval.

④ If the logic board is out of order, the LED will blink too fast or not be lit at all.

⑤ If no problems were found in the above examination, connect the logic main board with CN2003(13P), LY2000(40P), LE2001(40P), LE2002(40P), LE2003(40P), LG2001(40P), LG2002(40P) and LG2003(40P) using the connection cable.

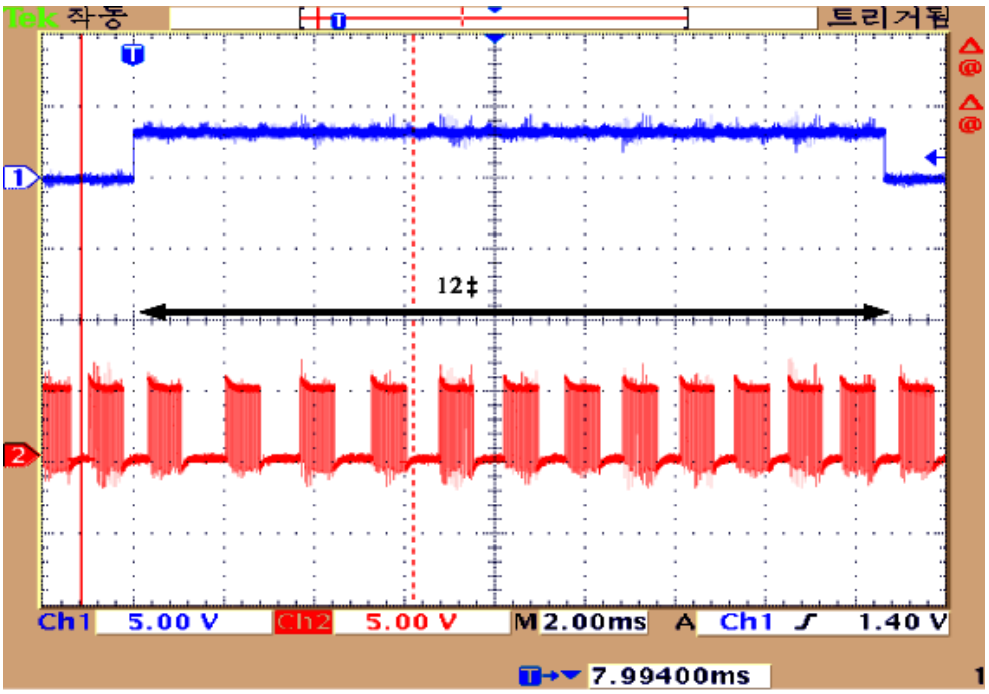
⑥ Set the oscilloscope at 4ms / div and 5V / div.

⑦ Check Drive Y s / w, Drive X s / w and the address signal in order.
Set Probe 1 of the oscilloscope to the trigger signal and connect it to TP41 of the logic board.

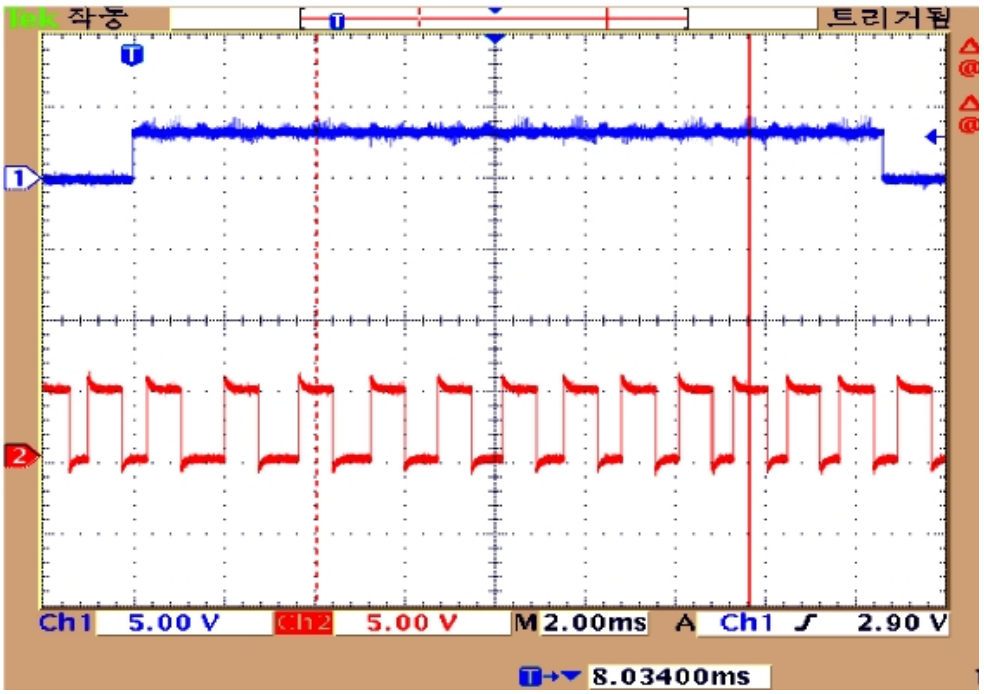
⑧ Measure the waveform at each test point on the board, and compare it with the appended waveforms. Make sure that you examine the waveforms of all the test points.

⑨ Turn off the power supply switch after the test, and disconnect the connector.

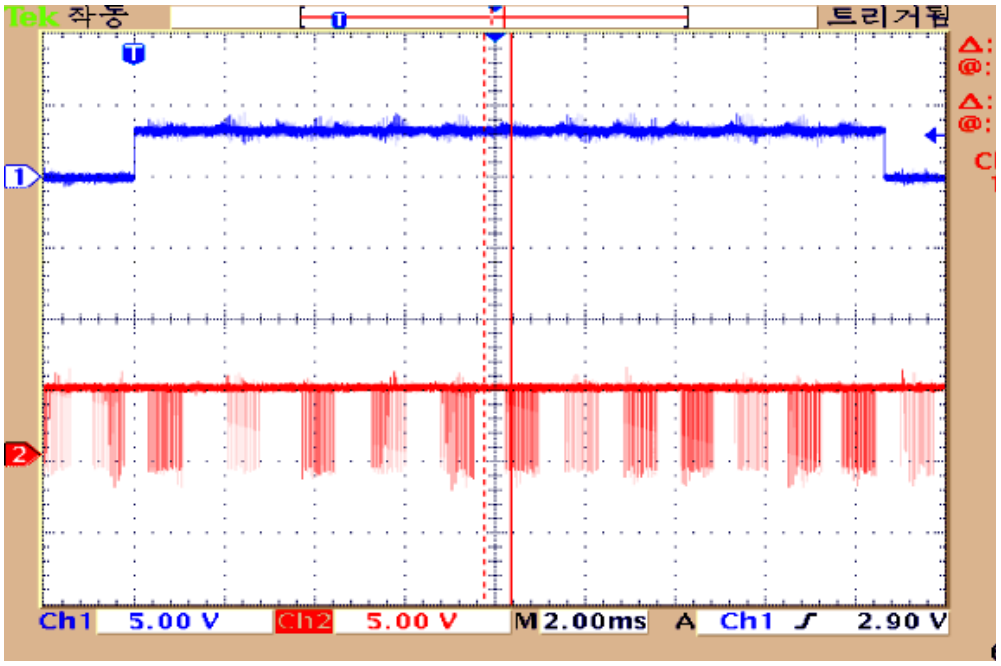
DATA(LE2001, LE2002, LE2003, LG2001, LG2002, LG2003 6~11, 15~20, 28~33
LG2003, LE2003 : 35~40)



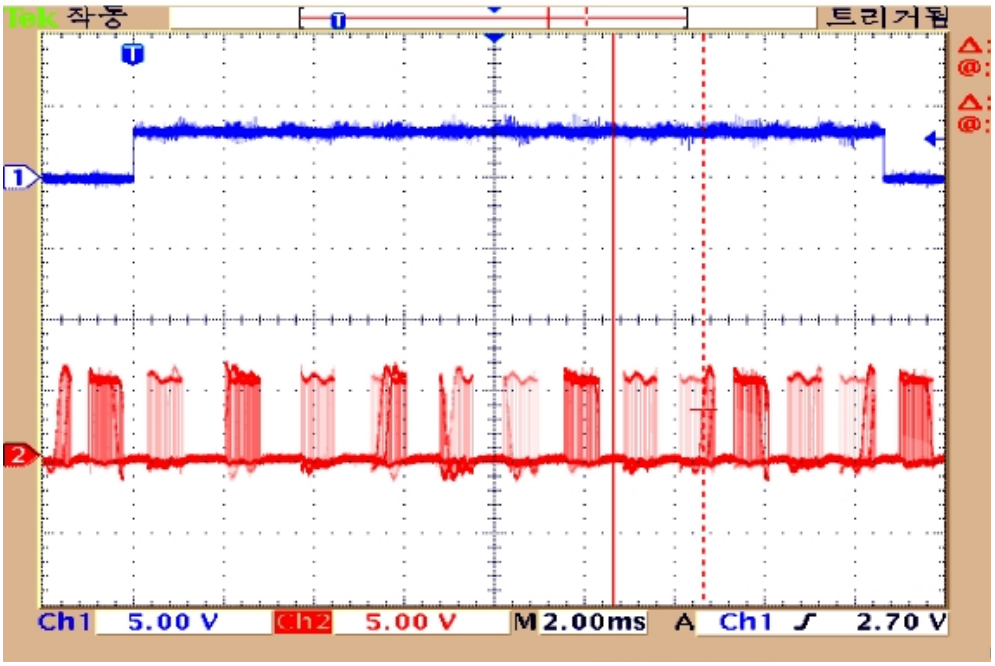
POL(LE2001, LE2002, LE2003, LG2001, LG2002, LG2003 : 25)



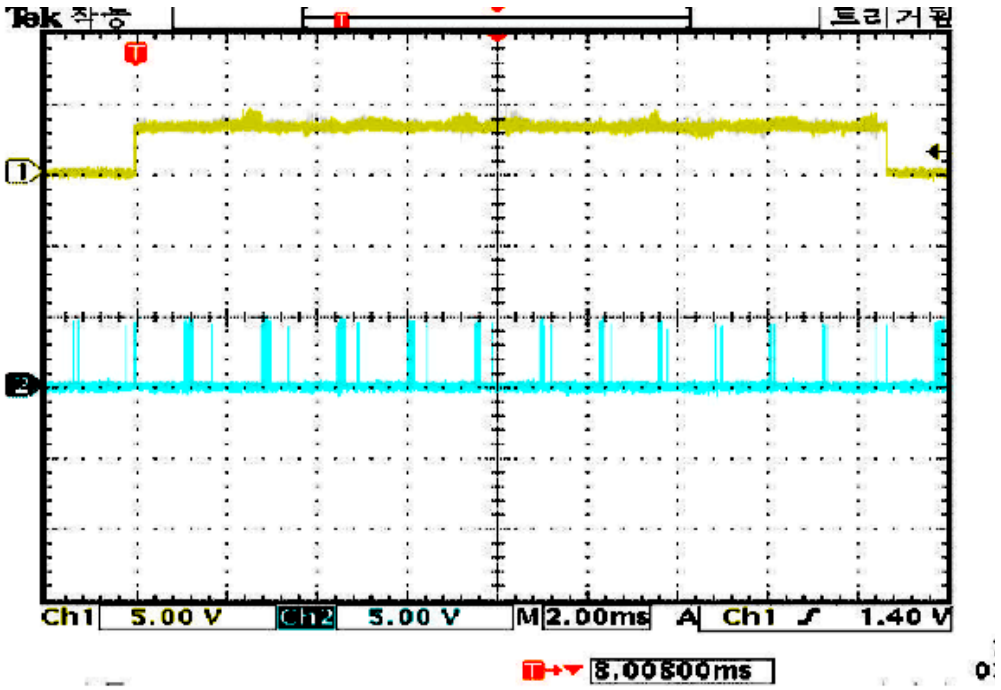
STB(LE2001, LE2002, LE2003, LG2001, LG2002, LG2003 : 24)



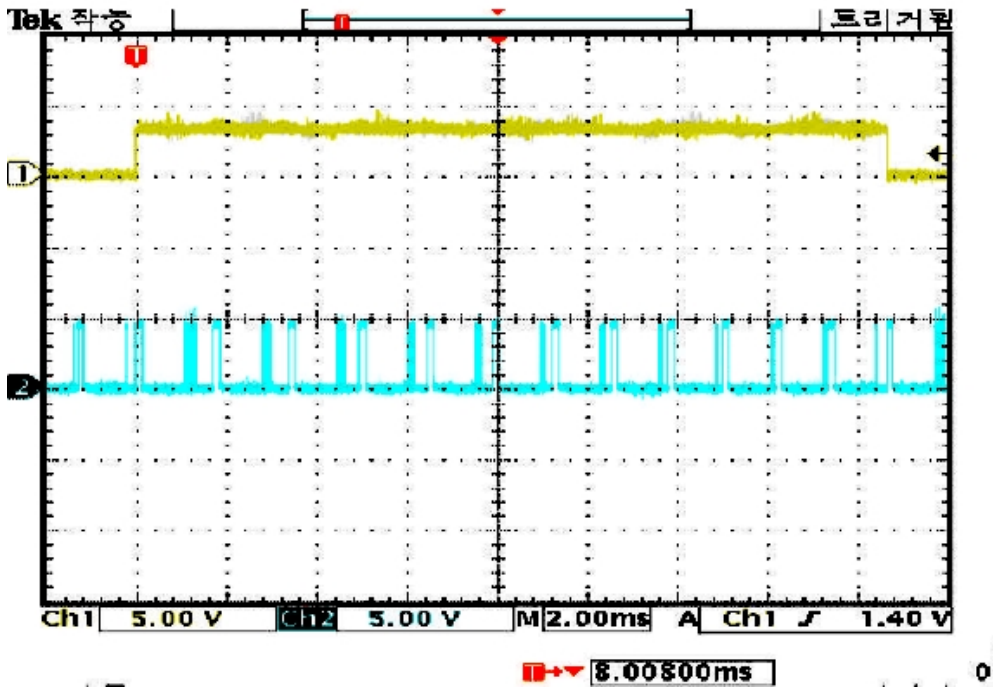
CLK(LE201, LE2002, LE2003, LG2001, LG2002, LG2003 : 13,22



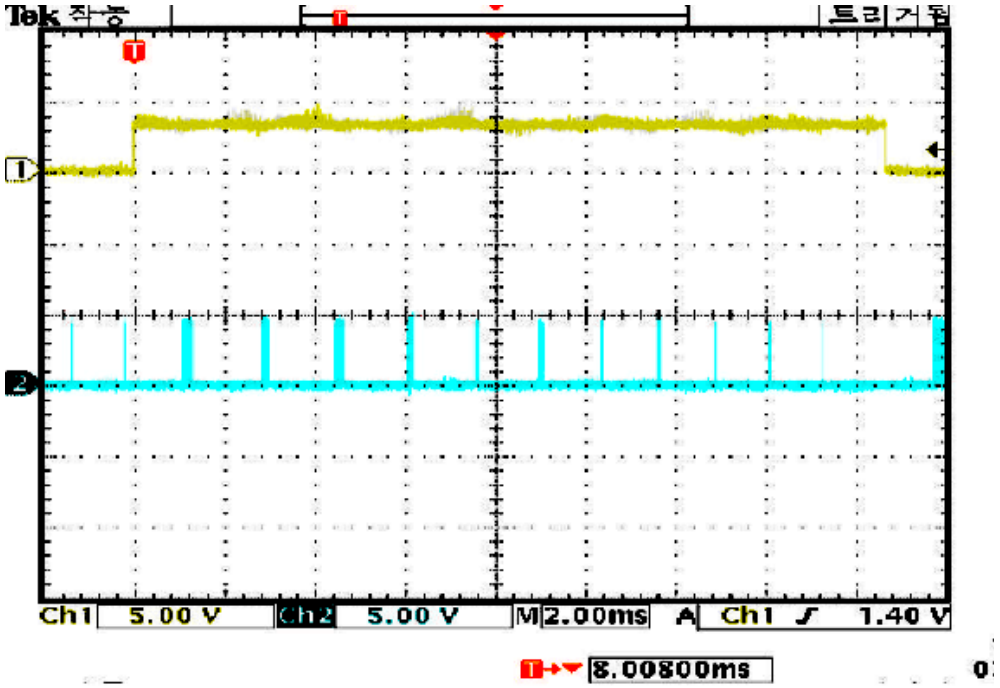
Y5


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

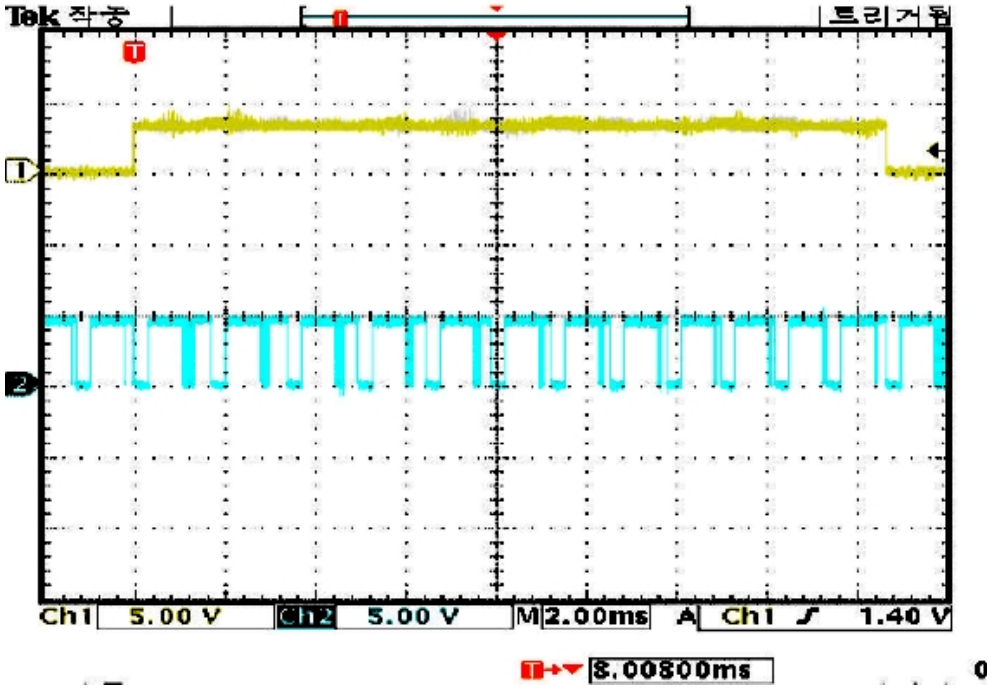
Y7


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

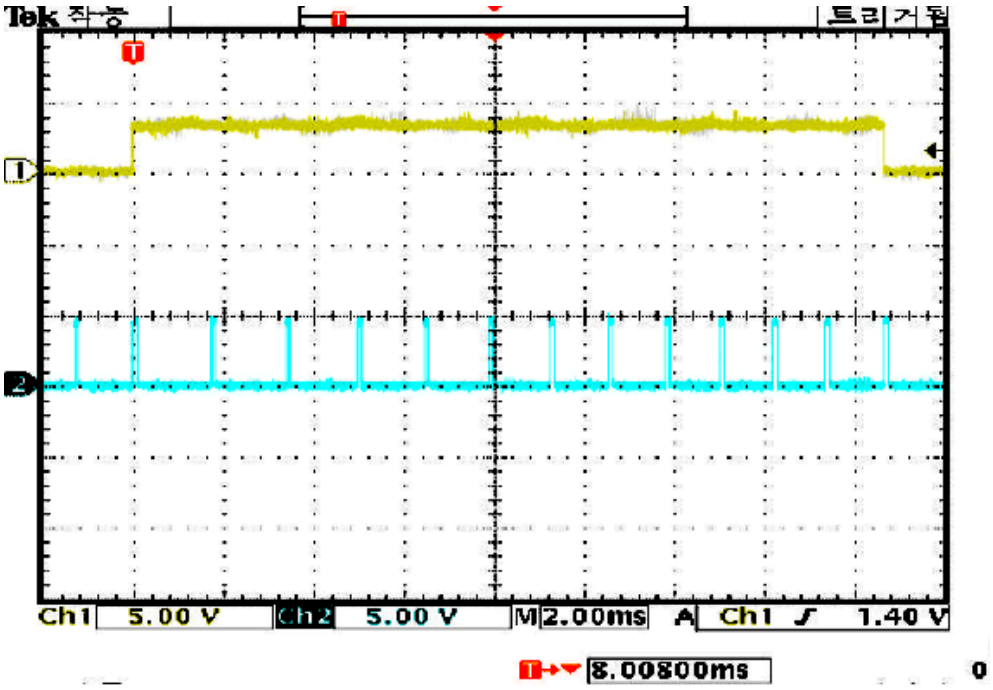
Y9


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

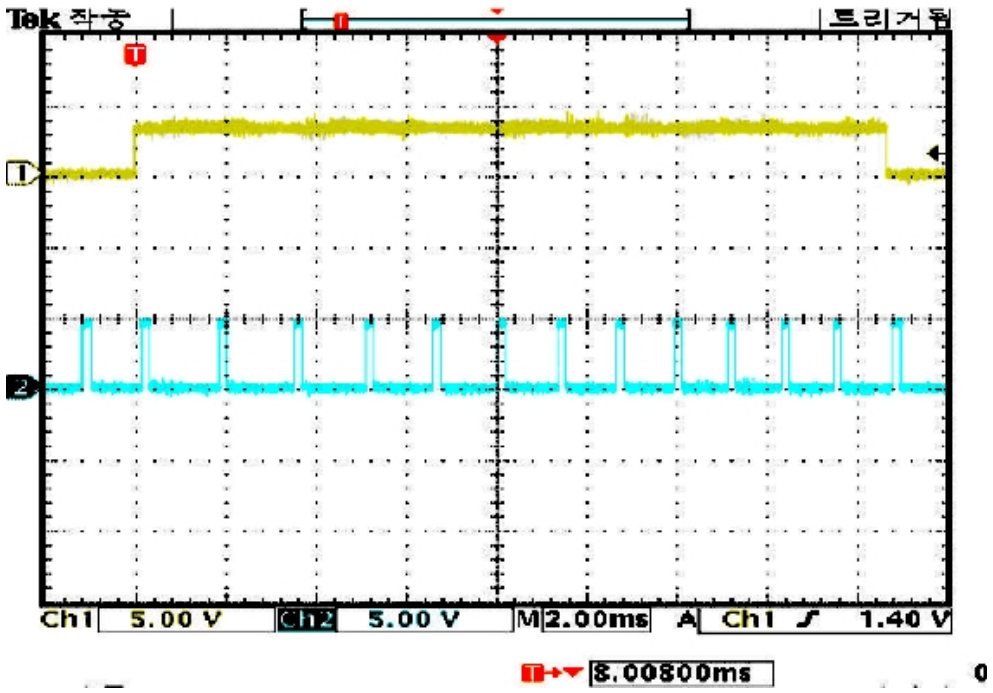
Y11


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

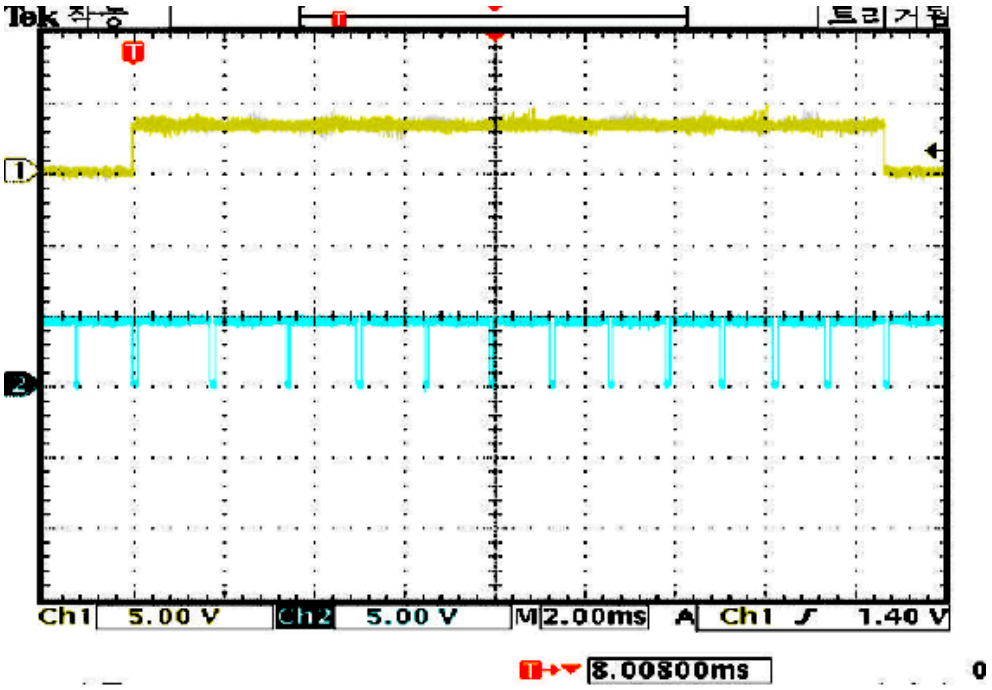
Y13


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

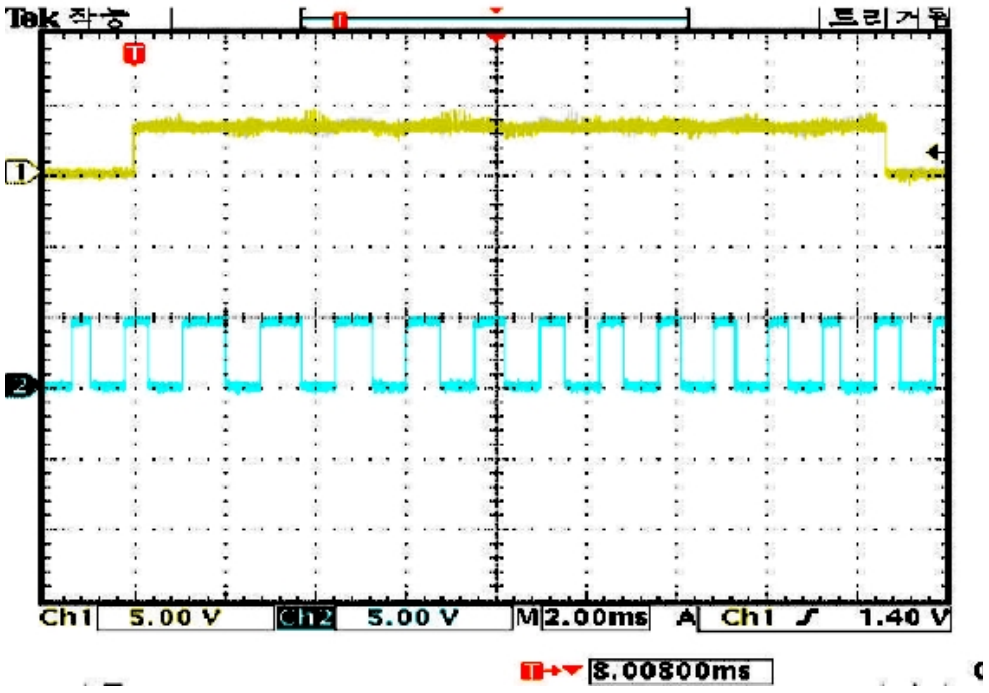
Y15


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

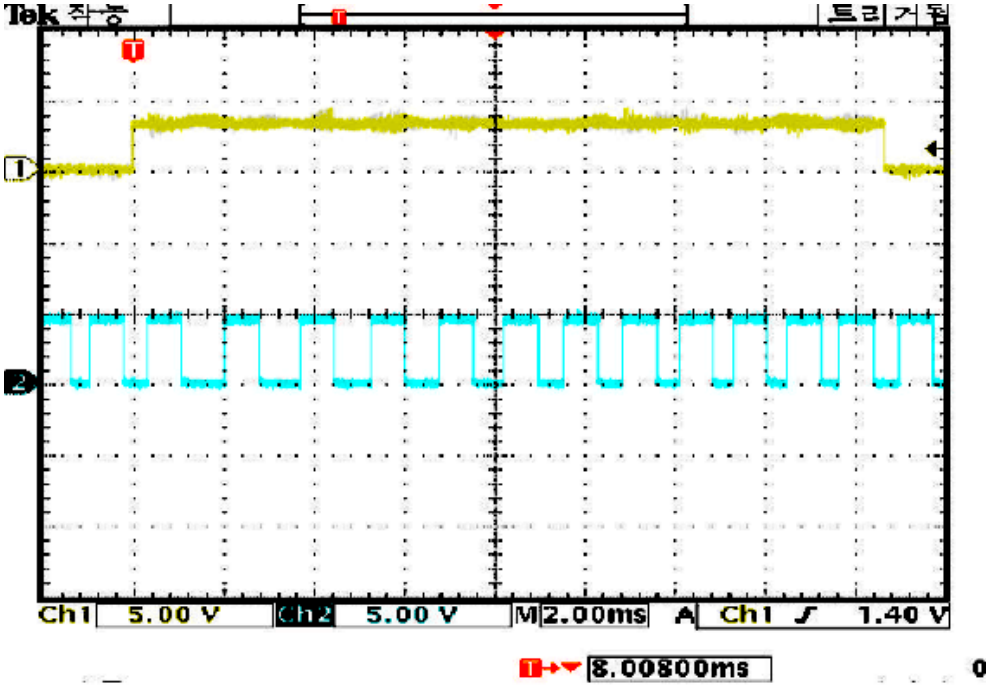
Y17


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

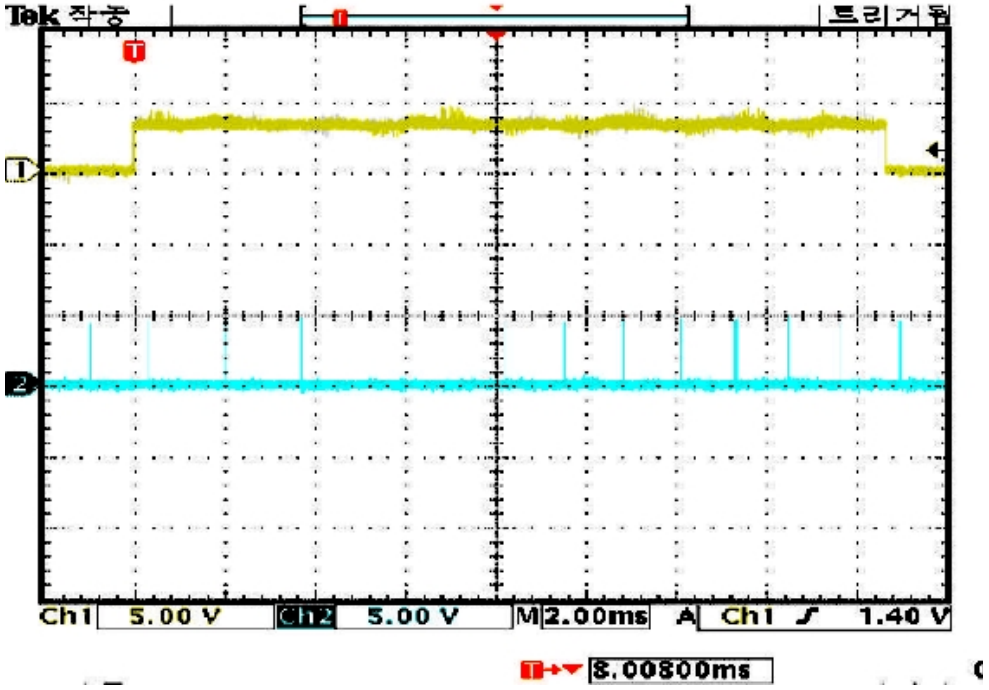
Y19


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

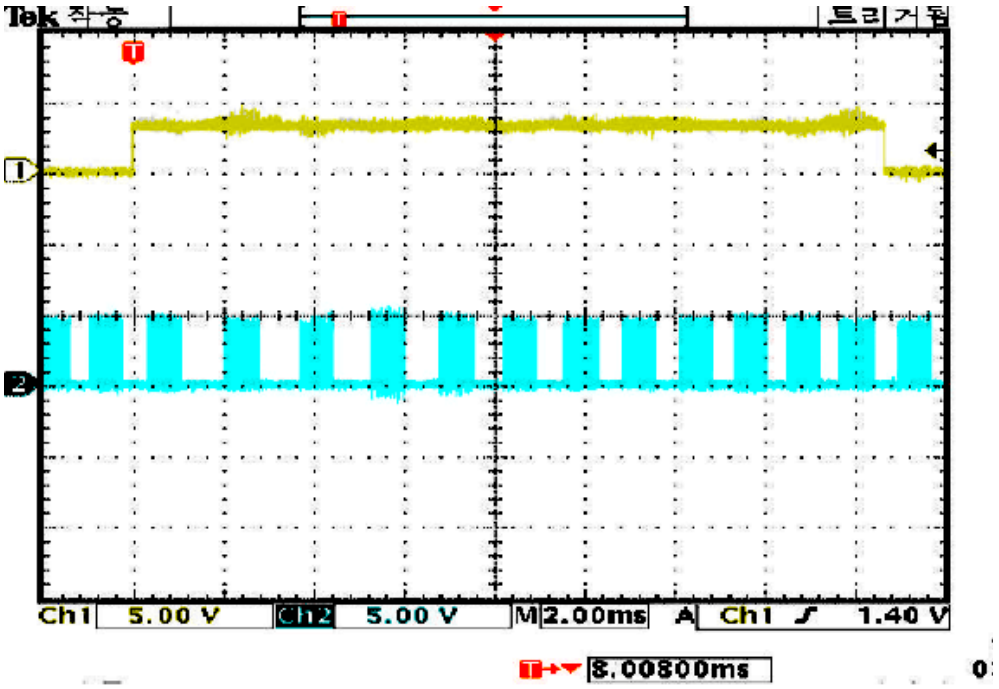
Y21


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

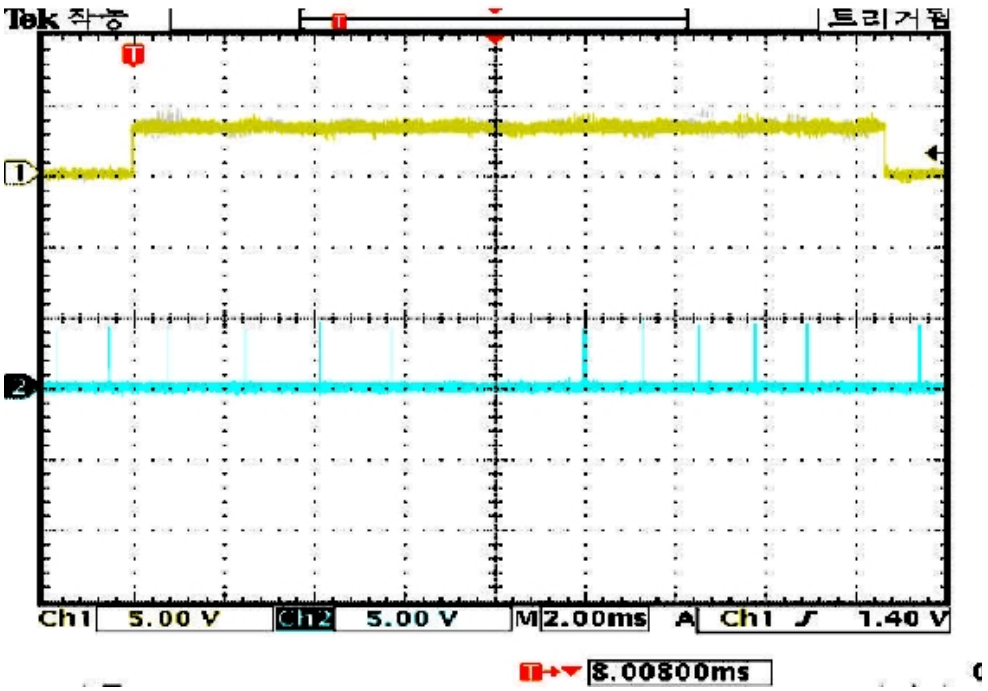
Y23


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

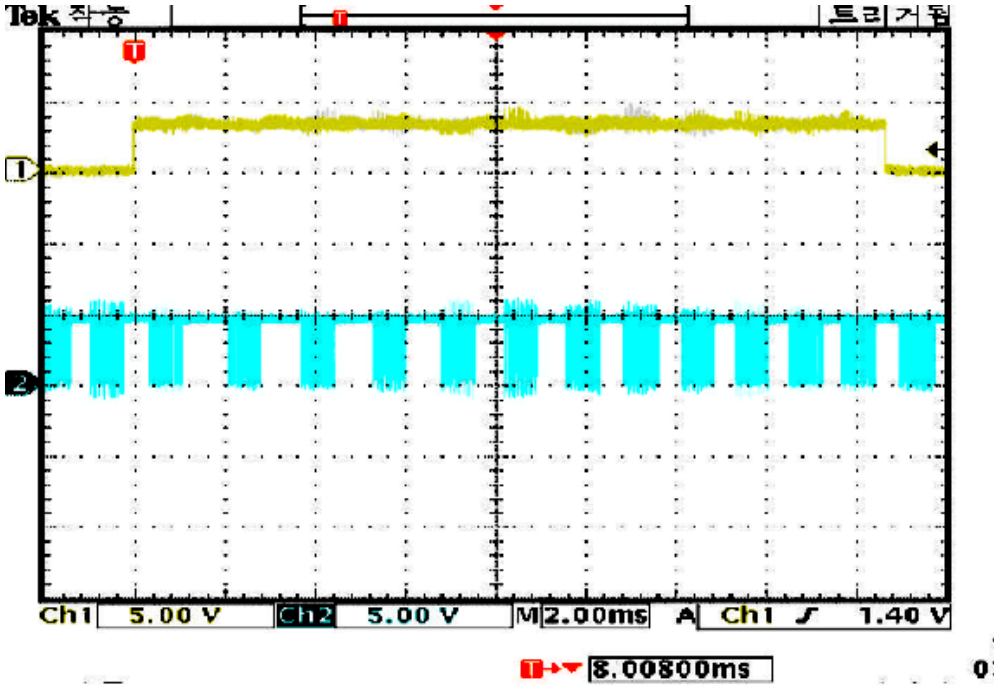
Y25


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

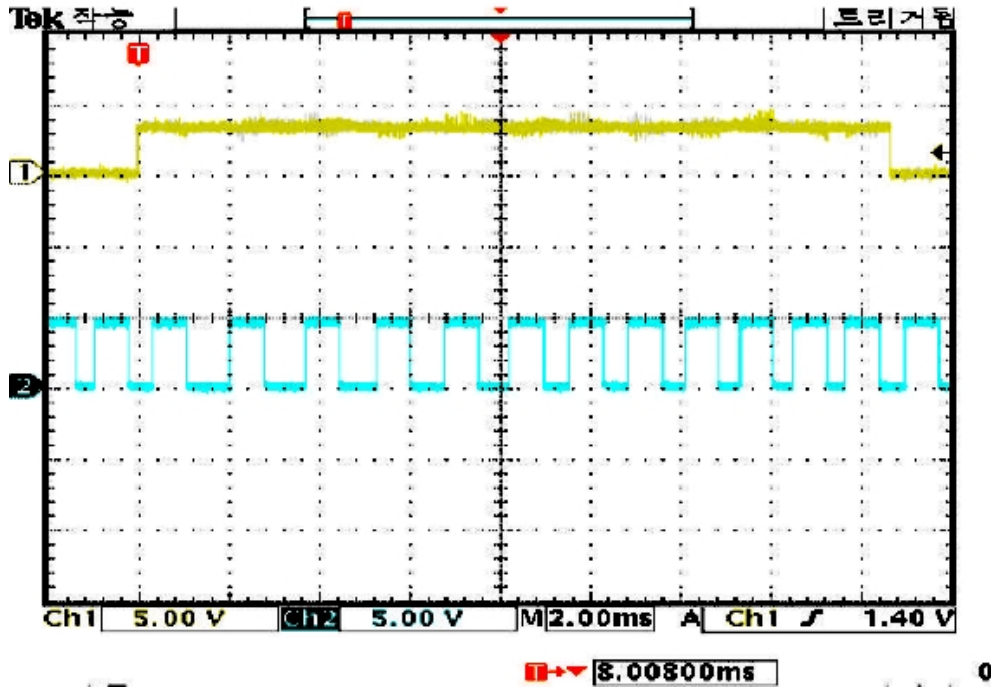
Y28


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

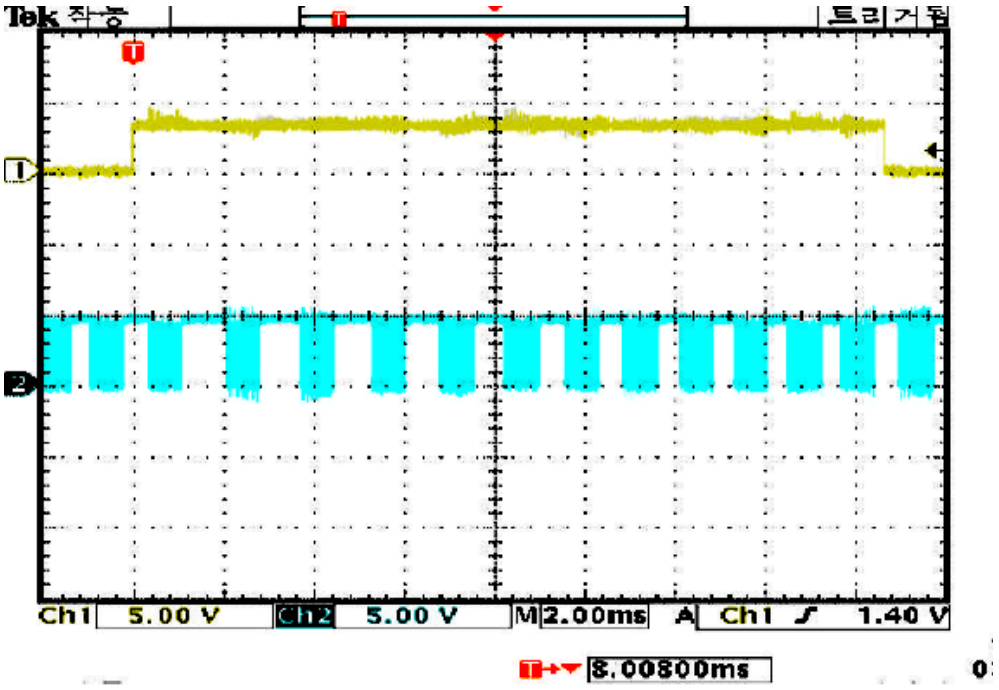
Y30


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

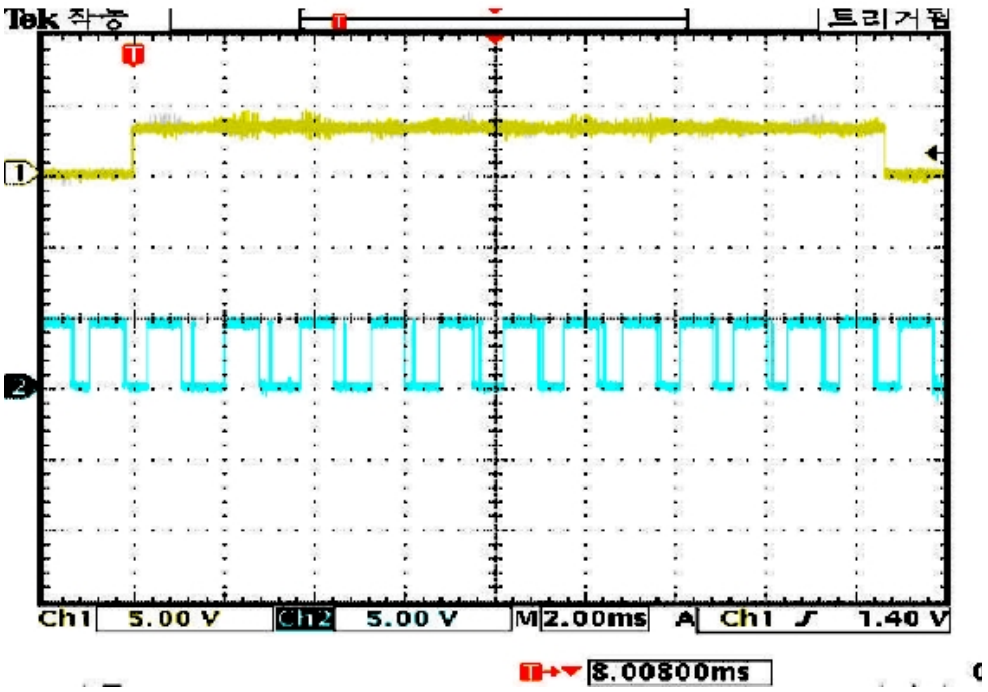
Y32


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

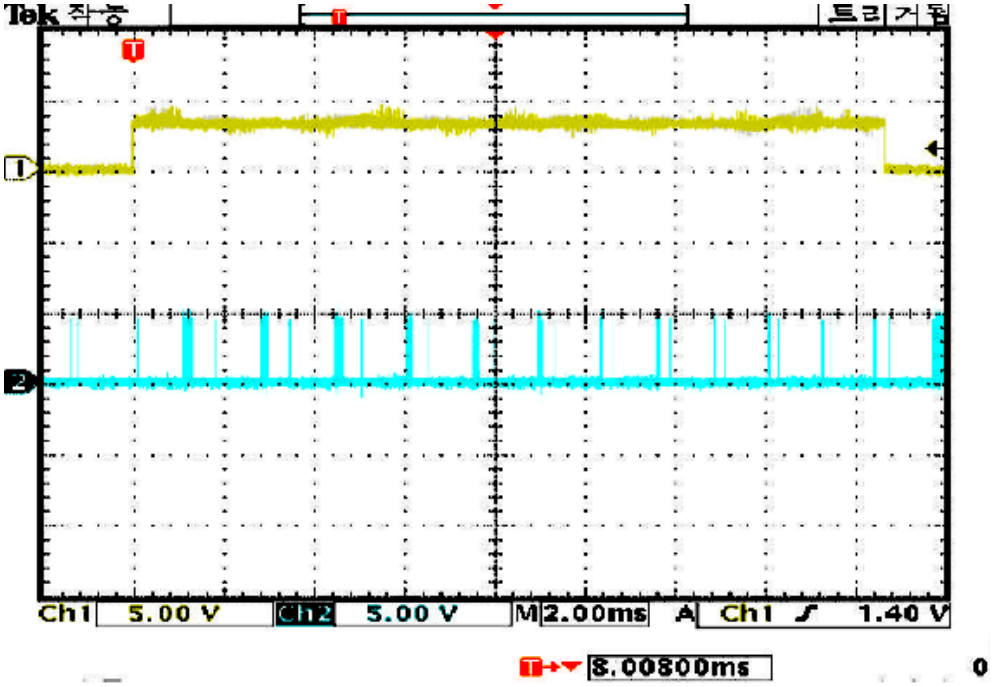
Y34


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

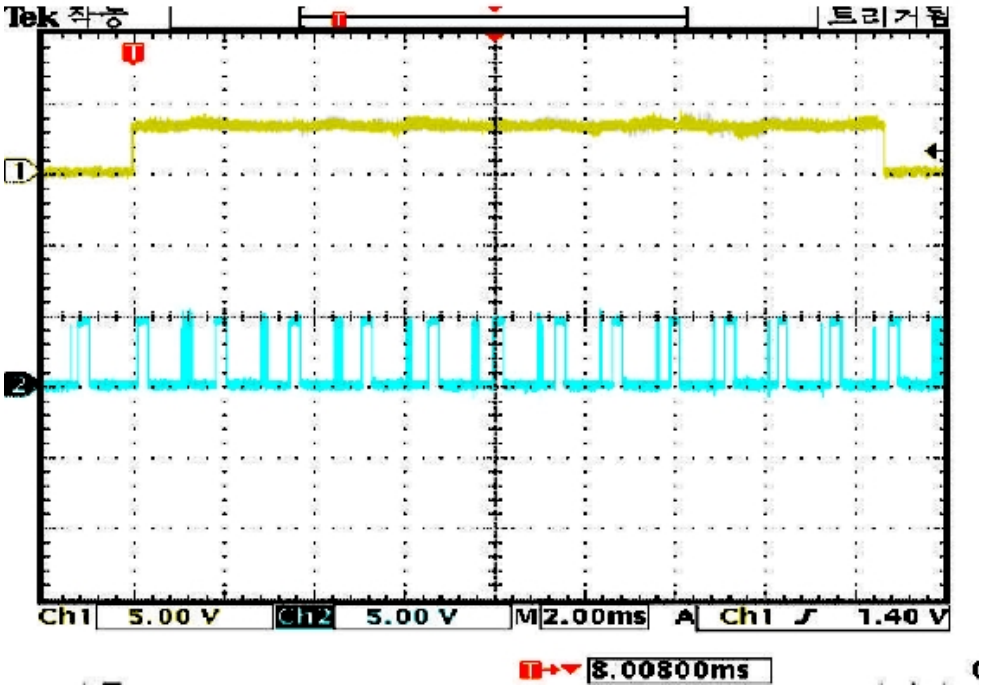
X2


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

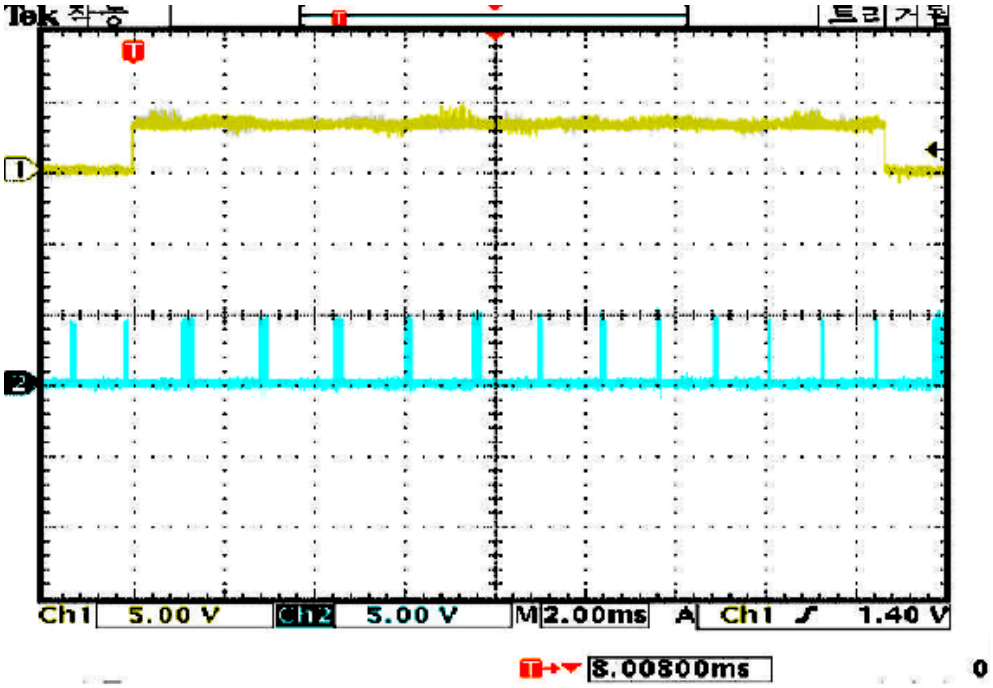
X4


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

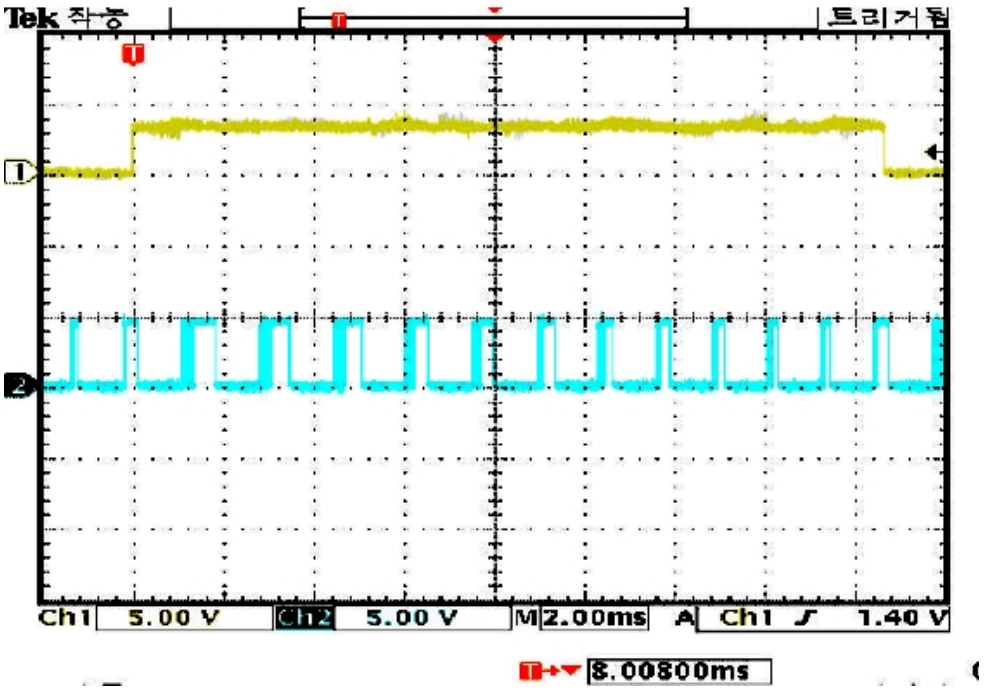
X6


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

X8


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

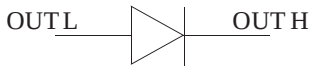
X10


Tek 작동
트리거됨
Ch1 5.00 V
Ch2 5.00 V
M 2.00ms
A Ch1 1.40 V
8.00800ms

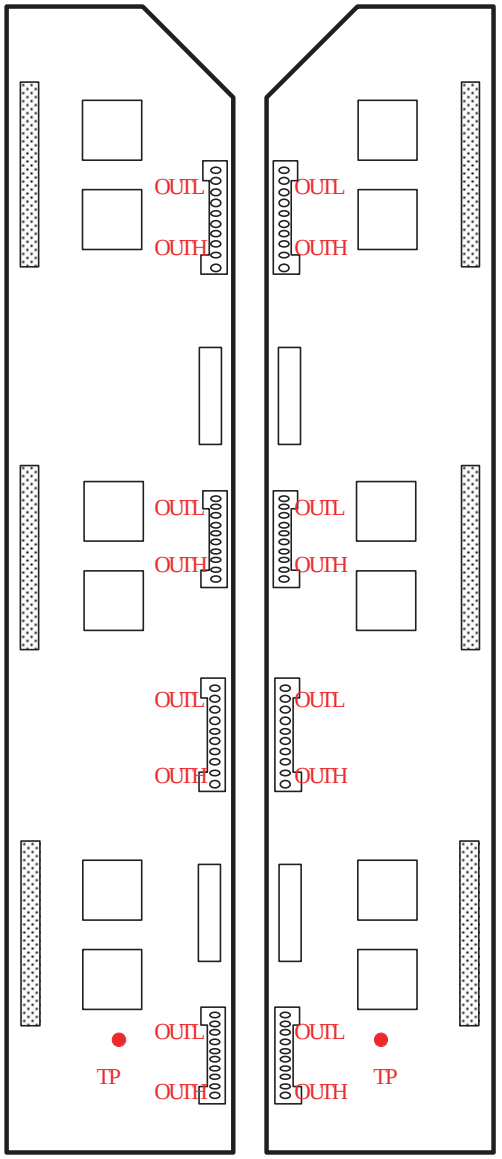
7-5 Inspection of the Driver Board

7-5-1 Y buffer

- To check if there is a problem with the Y main, first examine whether the Y buffer operates normally.
- Disconnect the connector between the Y main and the Y buffer.
- Diode-check the area between OUTL and OUTH to make sure that the flow of the voltage remains at 0.4V~0.5V.

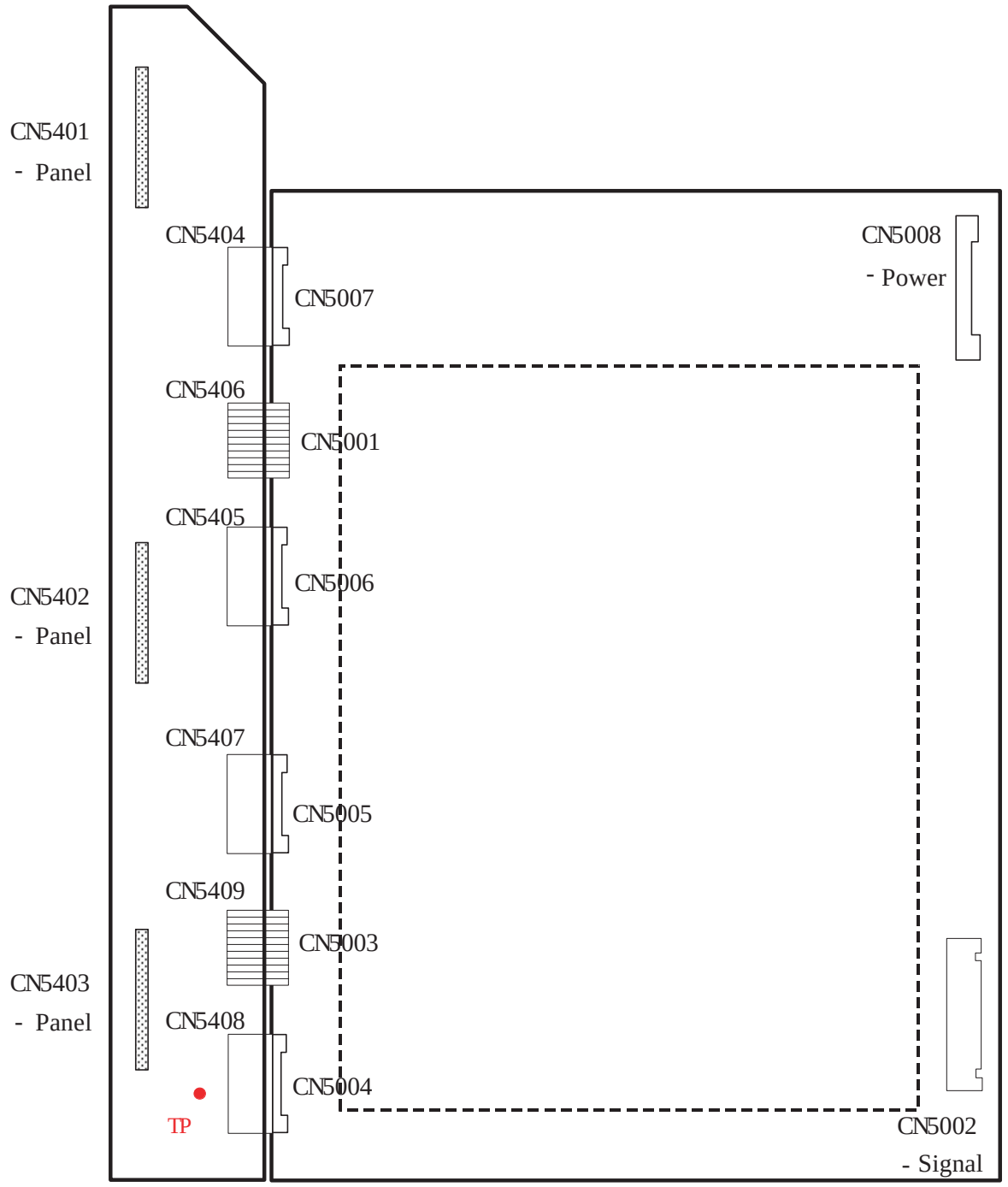


- The impedance between the two ends must be more than a few k Ω.



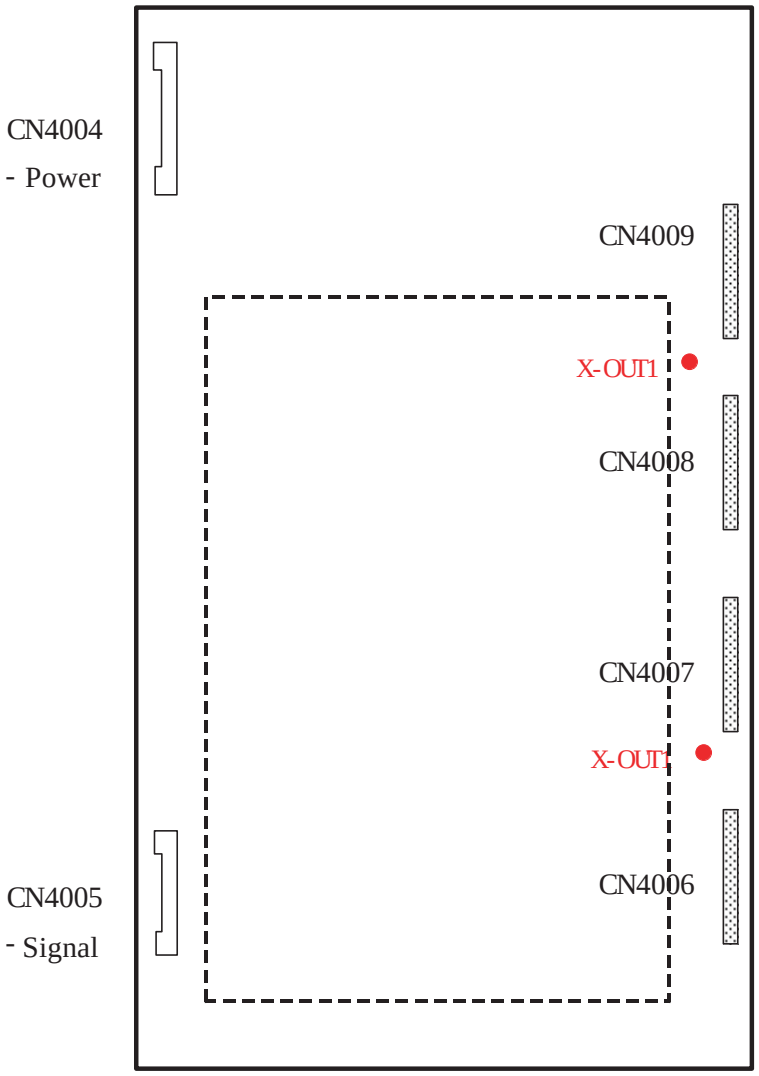
7-5-2 Y Main

- Connect the Y main to the Y buffer, and check that the output of the TP in the Y buffer appears as noted in Appendix 1 when power is applied.



7-5-3 X

-Check that the output of either Out 1 or Out 2 on the X board appears as noted in Appendix 2 when power is applied.

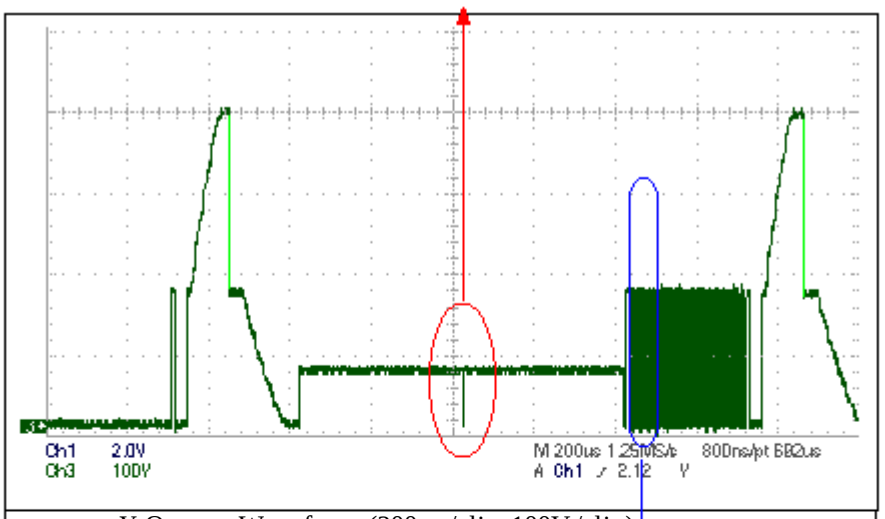


Appendix 1

■ Y Output Waveform

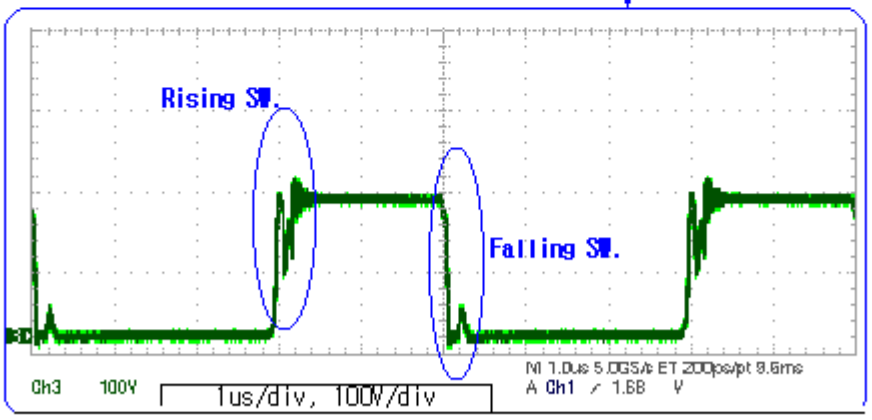
- The status of the waveform when it is not connected to the panel.

❉ Make sure there is only one scan waveform in the output!!



Y Output Waveform (200us / div, 100V / div)

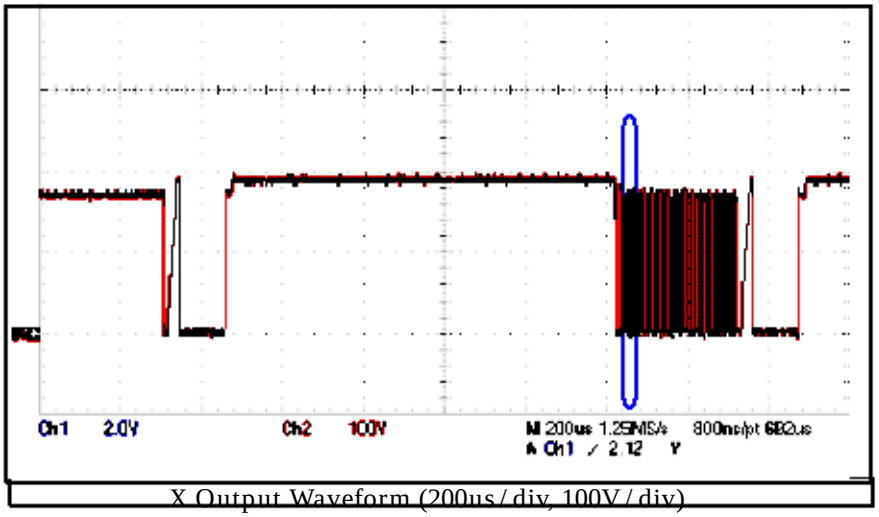
❉ Be sure to check that the energy recovery software is operating!!



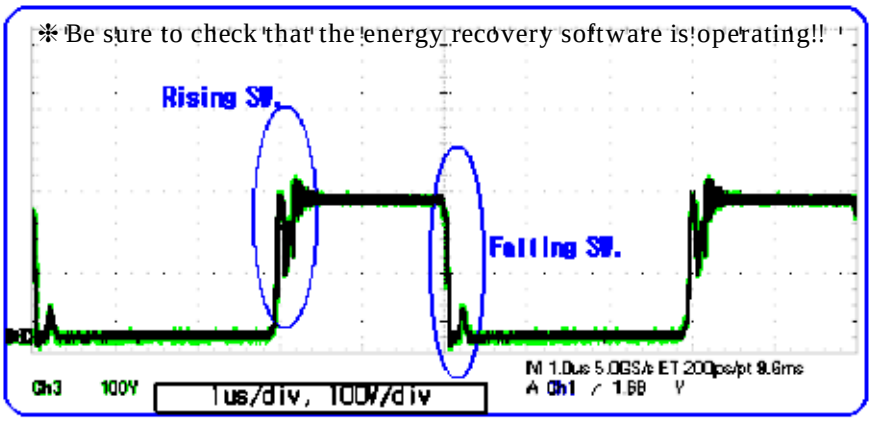
Appendix 2

■ X Output Waveform

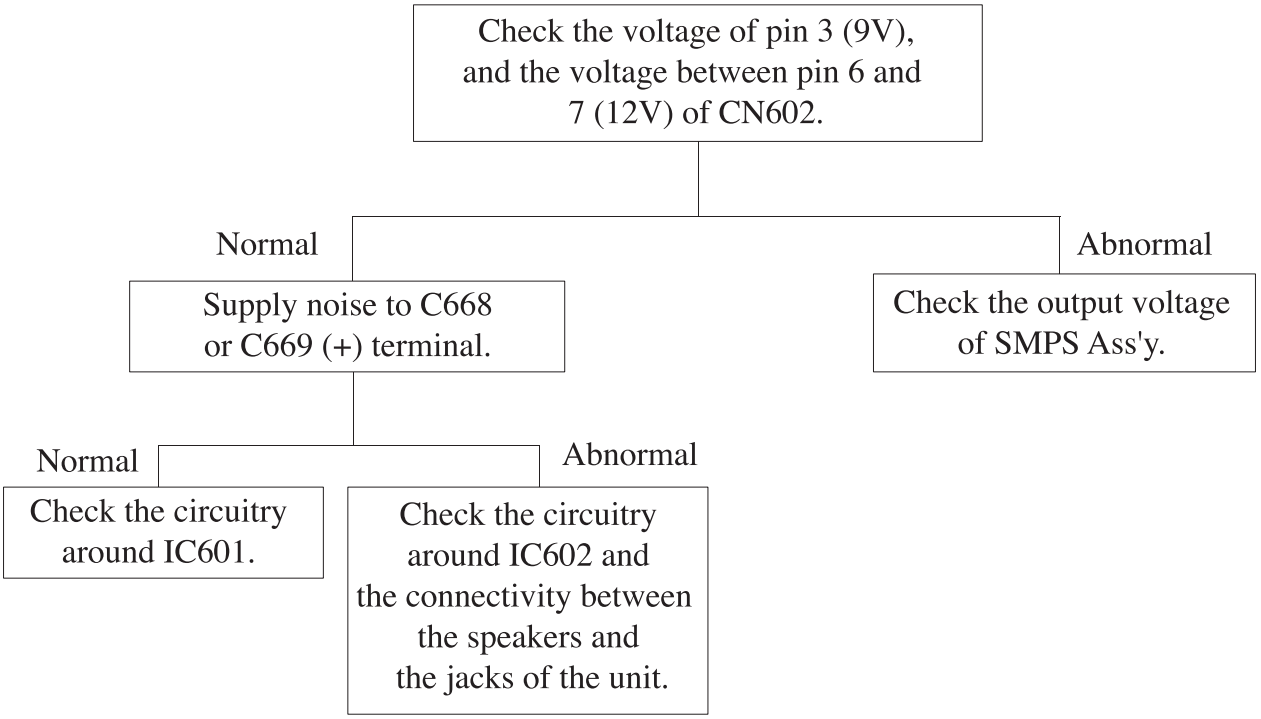
- The status of the waveform when it is not connected to the panel.



X Output Waveform (200us / div, 100V / div)



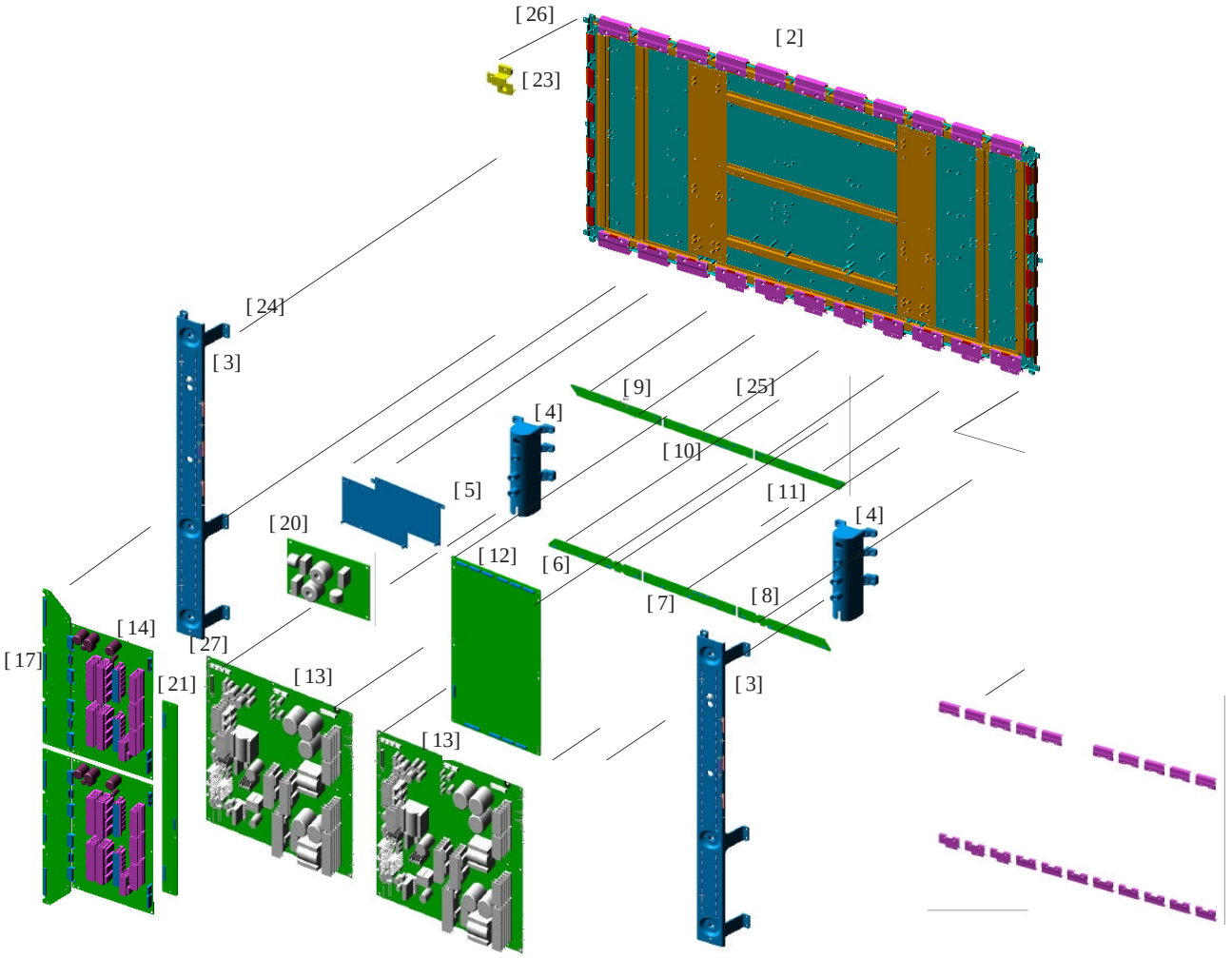
7-6 No audio is sounded and video is displayed properly



4. Exploded View and Parts List

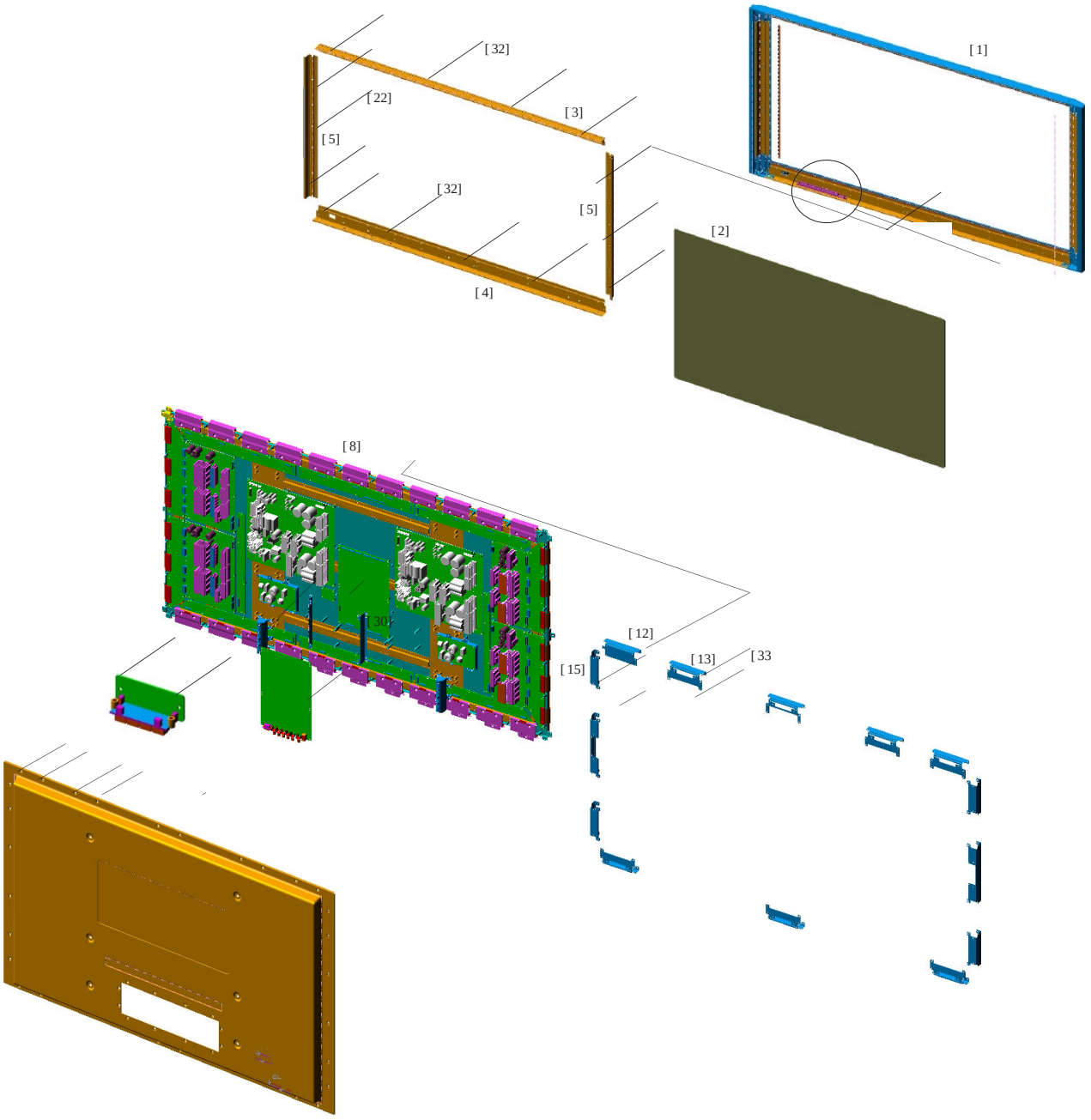
4-1 HPL63H1X/XAA MODULE

You can search for the updated part code through ITSELF web site.
URL : http://itself.sec.samsung.co.kr



NO	PART DESCRIPTION	CODE NO	SPECIFICATION	Q'TY
1	PANEL-PDP	DP63HW01A	63, HW,ASYM,DUAL, 300x340x380, 0~0, 1443x833	1
2	ASSY-CHASSIS, BASE	LJ93-00050A	63HD	1
3	BRACKET-WALL	LJ61-00714A	63HD, SECC, T2.0	2
4	GUIDE-STAND	LJ61-00552A	50HD,AL DIECASTING,	2
5	BRACKET-POWER	LJ61-00855A	63HD, SECC, T1.0, -, -, -, -	1
6	ASSY-PCB, BUFFER(E)	LJ92-00540B	63HD,LJ41-00940B, -, SDI, E-BUFFER, 438X45XT1.6MM,-, -,	1
7	ASSY-PCB, BUFFER(F)	LJ92-00541B	63HD,LJ41-00941B, -, SDI, F-BUFFER, 433X45XT1.6MM,-, -,	1
8	ASSY-PCB, BUFFER(G)	LJ92-00542B	63HD,LJ41-00942B, -, SDI, G-BUFFER, 438X45XT1.6MM,-, -,	1
9	ASSY-PCB, BUFFER(H)	LJ92-00543B	63HD,LJ41-00943B, -, SDI, H BUFFER, 438X45XT1.6MM,-, -,	1
10	ASSY-PCB, BUFFER(I)	LJ92-00544B	63HD,LJ41-00944B, -, SDI, I BUFFER, 433X45XT1.6MM,-, -,	1
11	ASSY-PCB, BUFFER(J)	LJ92-00545B	63HD,LJ41-00945B, -, SDI, J BUFFER, 438X45XT1.6MM,-, -,	1
12	ASSY-PCB, LOGIC(MAIN)	LJ92-00674A	63HD,LJ41-01057A, -, SDI, LOGIC MAIN, 320X190XT1.6MM,-	1
13	SMPS	LJ44-00039A	PDP-PS-63A, 110 ~ 130V, 47HZ-63HZ	2
14	ASSY-PCB, Y(MAIN)	LJ92-00603A	63HD,LJ41-01230A,63HD-YM1.0, SDI, Y MAIN, 315X190XT1	2
15	ASSY-PCB, X(MAIN)	LJ92-00552B	63HD,LJ41-01112A,63HD-XM1.0, SDI, X-MAIN, -, CLASS B,	2
16	ASSY-PCB, BUFFER(L)	LJ92-00547A	63HD,LJ41-00947A, -, SDI, Y-BUFFER LO,375X60XT1.6MM,-	1
17	ASSY-PCB, BUFFER(U)	LJ92-00546A	63HD,LJ41-00946A, -, SDI, Y-BUFFER UP,375X60XT1.6MM,-	1
18	ASSY-PCB, BUFFER(L)	LJ92-00549A	63HD,LJ41-00949A, -, SDI, X-BUFFER LO,375X60XT1.6MM,-	1
19	ASSY-PCB, BUFFER(U)	LJ92-00548A	63HD,LJ41-00948A, -, SDI, X-BUFFER UP,375X60XT1.6MM,-	1
20	ASSY-PCB, LINE(FILTER)	LJ92-00655A	63HD, -, -, SDI, AC LINE, 193.5X146XT1.6MM,-, -, -	1
21	ASSY-PCB, SUB	LJ92-00551A	63HD,LJ41-00951A, -, SDI, Y-SUB, 410X30X1.6MM,-, -, -	1
22	ASSY-PCB, SUB	LJ92-00550A	63HD,LJ41-00950A, -, SDI, X-SUB, 410X25X1.6MM,-, -, -	1
		LJ61-00520A	50HD, SECC, T1.0	1

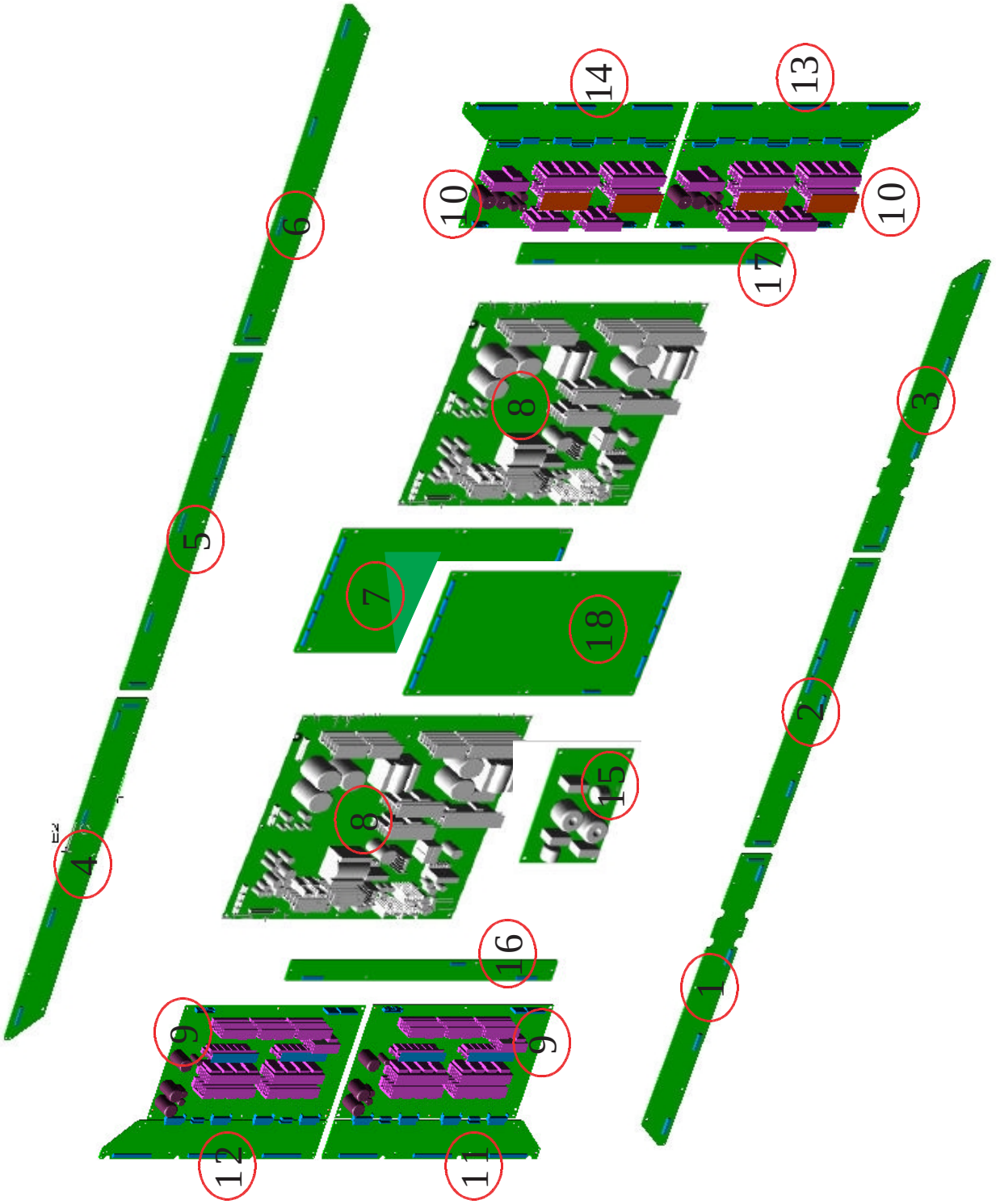
4-2 HPL63H1X/XAA MONITOR



NO	PART DESCRIPTION	CODE NO	SPECIFICATION	Q'TY
1	ASSY-CABINET, FRONT	LJ91-00472A	63HD, ABS, L/GRAY, SEC, -, -, -	1
2	GLASS-FILTER	LJ64-00052A	63HW/1363A-202S1-A, T3.8, W1442, L832, -, -, 0.1OHM	1
3	HOLDER-FITER, TOP	LJ61-00316B	63HD, AL, T1.5, -, L1422, -, -	1
4	HOLDER-FILTER, BOT	LJ61-00317B	63HD, AL, T1.5, -, L1422, -, -	1
5	HOLDER-FITER, SIDE	LJ61-00318B	63HD, AL, T1.5, -, L742, -, -	2
6	ASSY PCB CONTROL	LJ92-00538A	63HD, -, 63HD-KP-1.0, SDI, KEY PAD, 217X15XT1.6MM, -, -, -	1
7	BUTTON-CONTROL	LJ64-00030A	42"S1.0 ABS(V0)	1
8	MODULE	PM63HW003A	63, HW, ASYM, DUAL, 300x340x380, 0~0, 1443x833	1
9	ASSY-PCB, VIDEO	LJ92-00592A	63HD, -, -, SDI, SCALER BOARD, -, D52A, HPL5025M, -, -	1
10	ASSY-PCB, TERMINAL	LJ92-00586B	63HD, -, 63HD-ST-1.0, SDI, SDI, SPK TERM, -, CLASS B, -, -	1
11	ASSY-PCB, AUDIO	LJ92-00593A	63HD, -, -, SDI, AUDIO SOUND, -, HPL5025MK/XAA, D52A, -, -	1
12	HOLDER-CABINET, TL	LJ61-00733A	63HD, SPC, T1.6, -, -, -, -	1
13	HOLDER-CABINET	LJ61-00715A	63HD, SPC, T1.6, -, -, -, NI	6
14	HOLDER-CABINET, TM	LJ61-00789A	50HD, SPC, T1.6, -, -, -, -	1
15	HOLDER-CABINET, SIDE	LJ61-00734A	63HD, SPC, T1.6, -, -, -, -	2
16	HOLDER-CABINET, SIDE(M)	LJ61-00735A	63HD, SPC, T1.6, -, -, -, -	2
17	BRACKET-RMC	LJ61-00324A	SPD-42P1S, SECC, T1.0, -, -, -, -	1
18	ASSY PCB CONTROL	LJ92-00539A	63HD, -, 63HD-RM1.0, SDI, R/MODULE, 90X27X1.6MM, -, -, -	1
19	COVER-BACK, TERMIAL	LJ63-01065A	63HD, AL, T1.5, -, -, -, -, BLK, -	1
20	COVER-BACK	LJ63-01064B	63HD, AL, T1.5, -, -, -, -, BLK, -	1
21	SCREW-ASS'Y, MACH	6006-001035	WSP, PH, +, M3, L8, ZPC(YEL), SM10C	1
22	SCREW-TAPPING	6002-001142	TH, +, 2, M3.5, L10, ZPC(YEL), SWRCH18A	1
	SCREV-MACHINE	6001-000667	PVF, +, M3, L8, ZPC(YEL), SM20C, -	3

4-3 For assy replacement, code number and description by assy

In order to replace a broken part, please see the figure below and makea request using the assy code number of a spec assy neccessary for replacement.

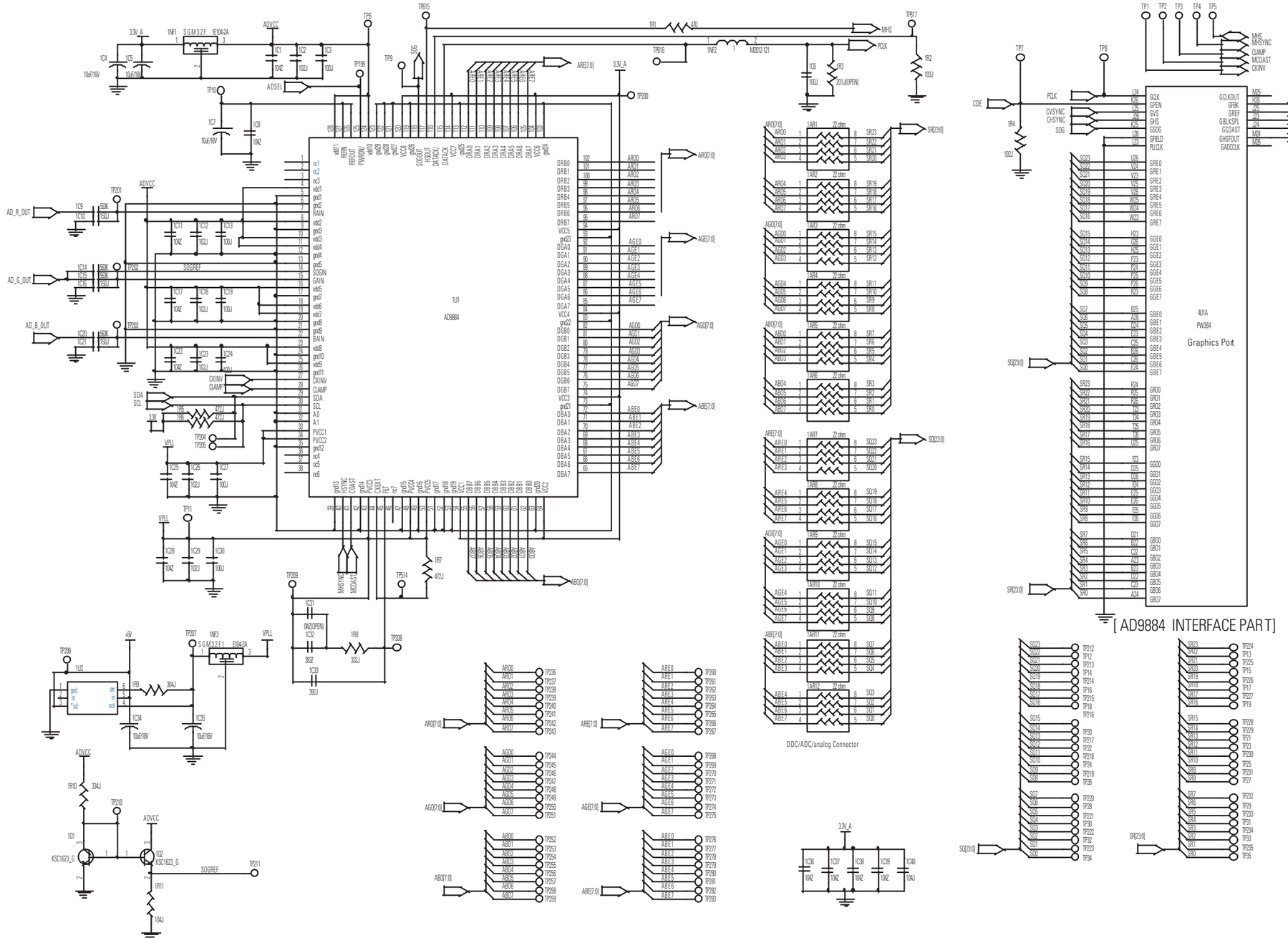


NO	PART DESCRIPTION	CODE NO	SPECIFICATION	Q'TY
1	ASSY-PCB,BUFFER(E)	LJ92-00540B	63HD,LJ41-00940B,-,SDI,E-BUFFER,438X45XT1.6MM,-,-,	1
2	ASSY-PCB,BUFFER(F)	LJ92-00541B	63HD,LJ41-00941B,-,SDI,F-BUFFER,433X45XT1.6MM,-,-,	1
3	ASSY-PCB,BUFFER(G)	LJ92-00542B	63HD,LJ41-00942B,-,SDI,G-BUFFER,438X45XT1.6MM,-,-,	1
4	ASSY-PCB,BUFFER(H)	LJ92-00543B	63HD,LJ41-00943B,-,SDI,H BUFFER,438X45XT1.6MM,-,-,	1
5	ASSY-PCB,BUFFER(I)	LJ92-00544B	63HD,LJ41-00944B,-,SDI,I BUFFER,433X45XT1.6MM,-,-,	1
6	ASSY-PCB,BUFFER(J)	LJ92-00545B	63HD,LJ41-00945B,-,SDI,J BUFFER,438X45XT1.6MM,-,-,	1
7	ASSY-PCB,LOGIC(MAIN)	LJ92-00674A	63HD,LJ41-01057A,-,SDI,LOGIC MAIN,320X190XT1.6MM,-	1
8	SMPS	LJ44-00039A	PDP-PS-63A,110 ~ 130V,47HZ-63HZ	2
9	ASSY-PCB,Y(MAIN)	LJ92-00603A	63HD,LJ41-01230A,63HD-YM1.0,SDI,Y MAIN,315X190XT1	2
10	ASSY-PCB,X(MAIN)	LJ92-00552B	63HD,LJ41-01112A,63HD-XM1.0,SDI,X-MAIN,-,CLASS B,	2
11	ASSY-PCB,BUFFER(L)	LJ92-00547A	63HD,LJ41-00947A,-,SDI,Y-BUFFER LO,375X60XT1.6MM,-	1
12	ASSY-PCB,BUFFER(U)	LJ92-00546A	63HD,LJ41-00946A,-,SDI,Y-BUFFER UP,375X60XT1.6MM,-	1
13	ASSY-PCB,BUFFER(L)	LJ92-00549A	63HD,LJ41-00949A,-,SDI,X-BUFFER LO,375X60XT1.6MM,-	1
14	ASSY-PCB,BUFFER(U)	LJ92-00548A	63HD,LJ41-00948A,-,SDI,X-BUFFER UP,375X60XT1.6MM,-	1
15	ASSY-PCB,LINE(FILTER)	LJ92-00655A	63HD,-,-,SDI,AC LINE ,193.5X146XT1.6MM,-,-,-	1
16	ASSY-PCB,SUB	LJ92-00551A	63HD,LJ41-00951A,-,SDI,Y-SUB,410X30X1.6MM,-,-,-	1
17	ASSY-PCB,SUB	LJ92-00550A	63HD,LJ41-00950A,-,SDI,X-SUB,410X25X1.6MM,-,-,-	1
18	ASSY PCB VIDEO	LJ92-00592A	63HD,-,-,SDI,SCALER BOARD,-,D52A,HPL5025M	

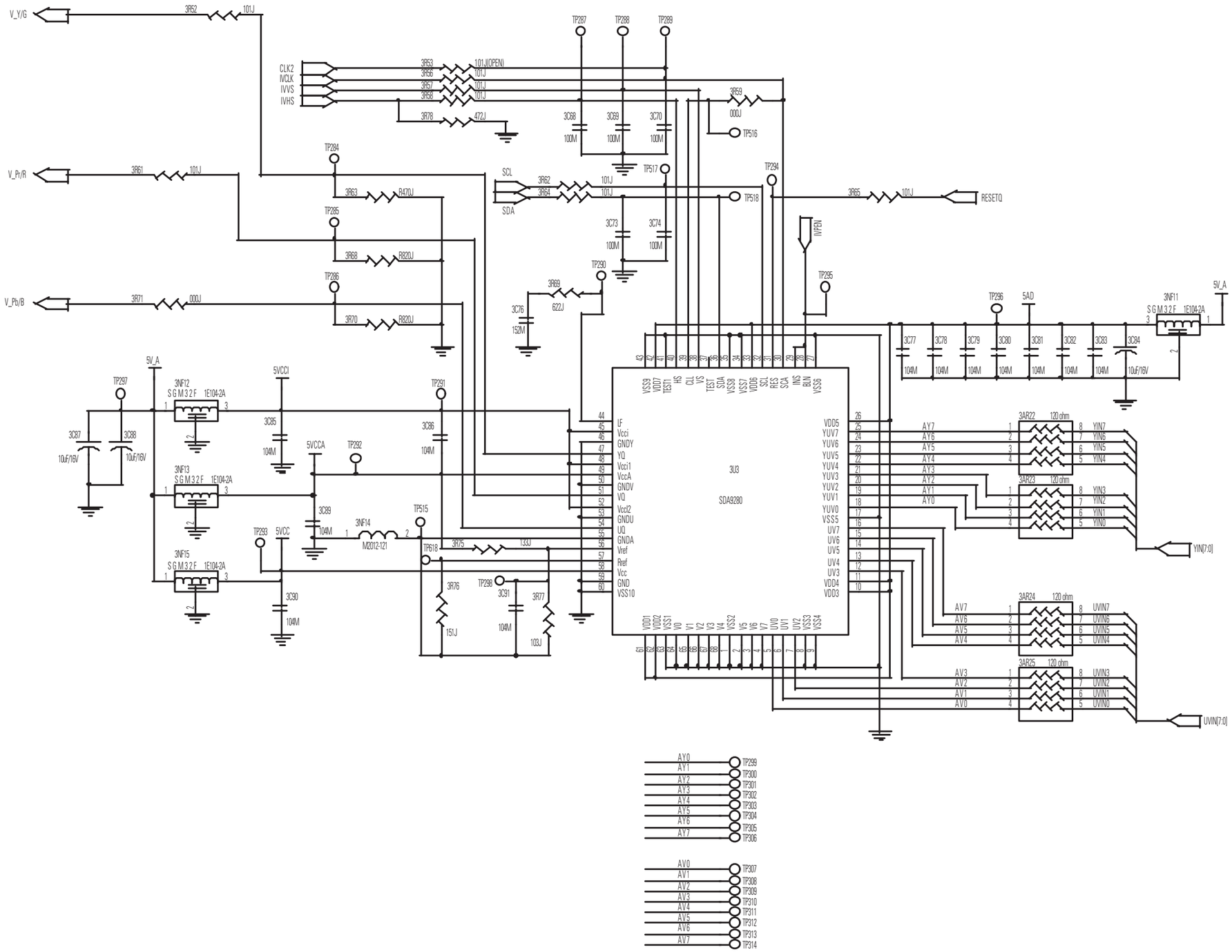
10. Schematic Diagrams

10-1 VIDEO

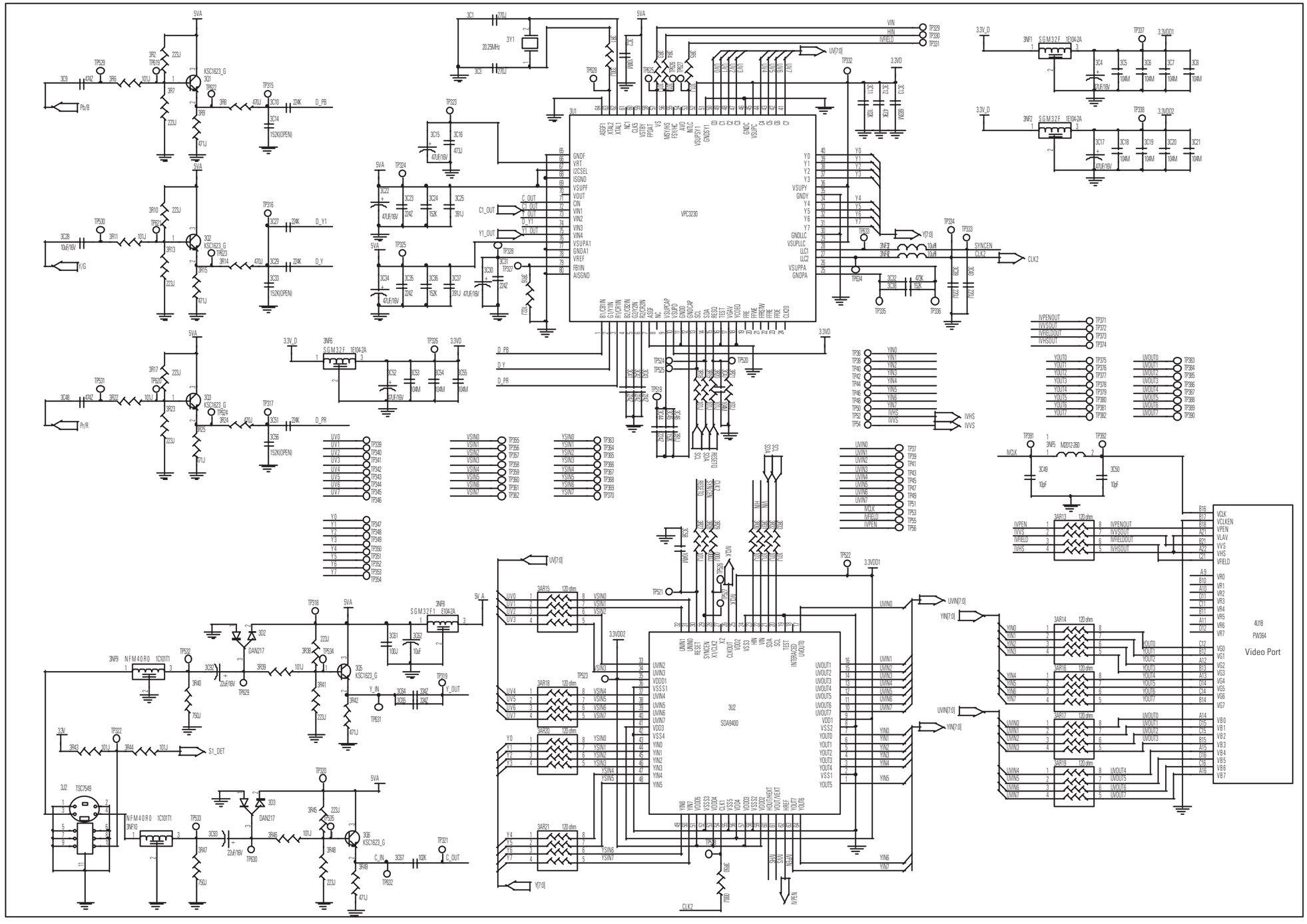
10-1-1 MAIN ADC (AD9884)



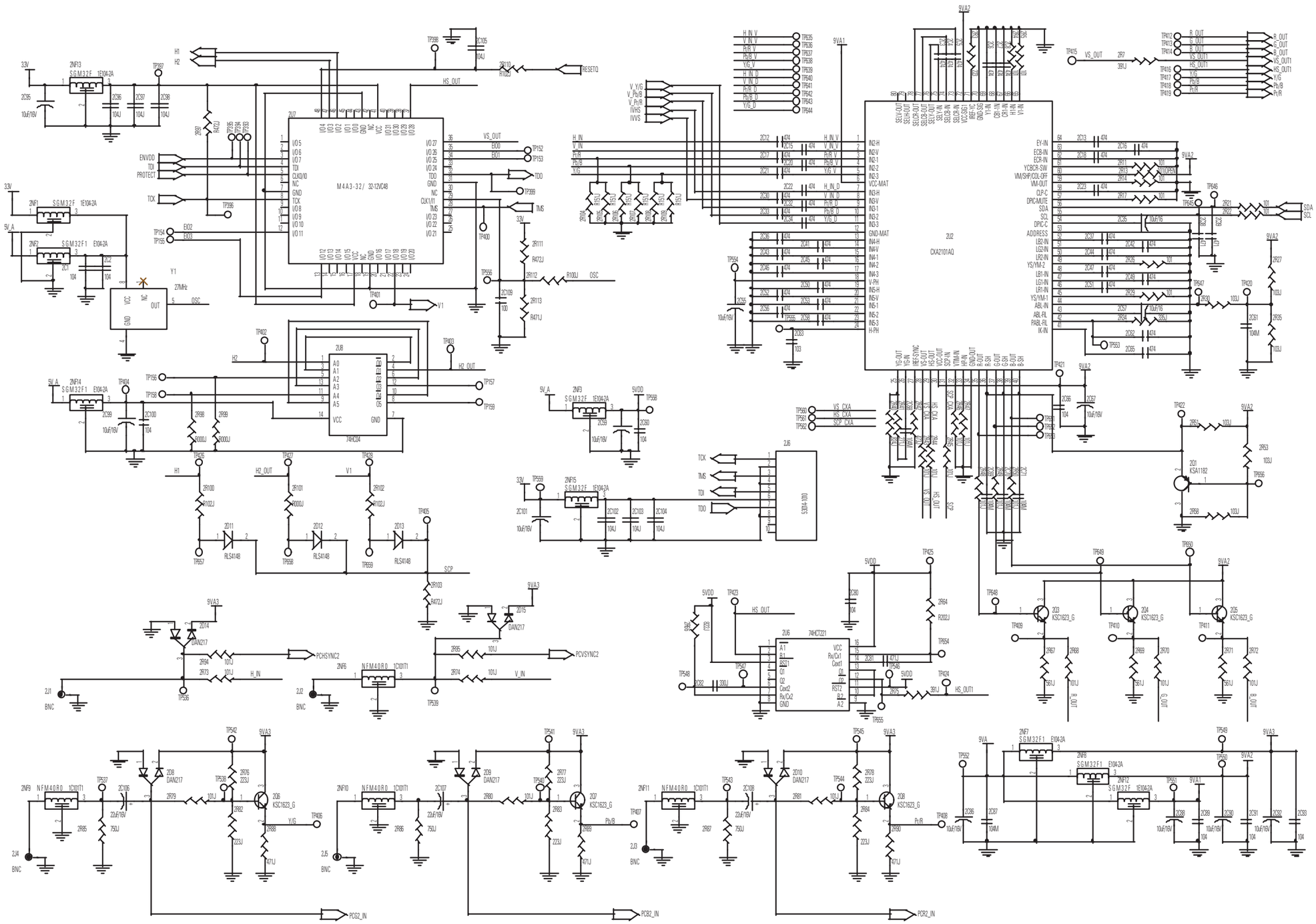
10-1-2 VIDEO D/A CONVERTER



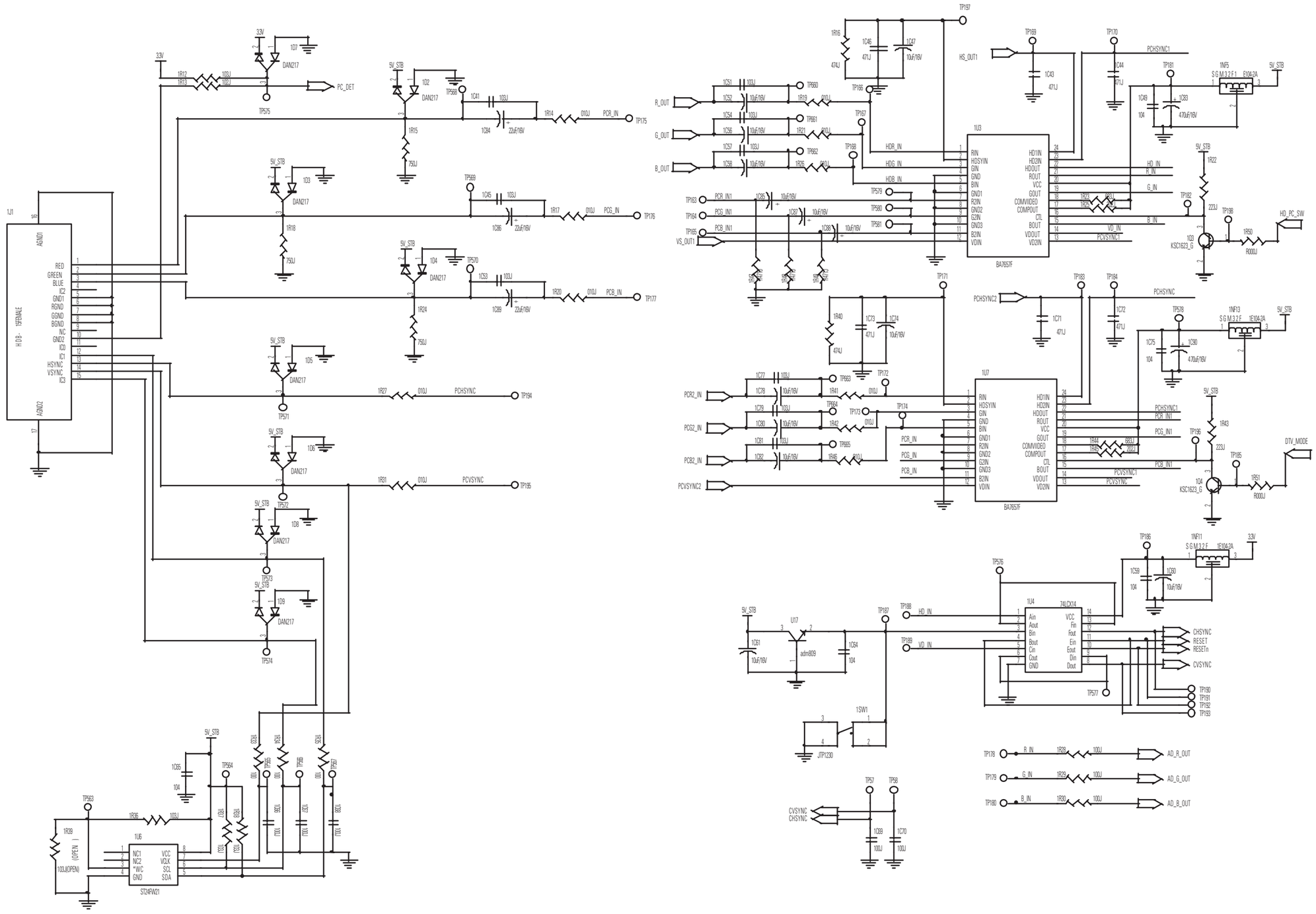
10-1-3 S-VIDEO &COMPONENT1 SIGNAL PROCESS



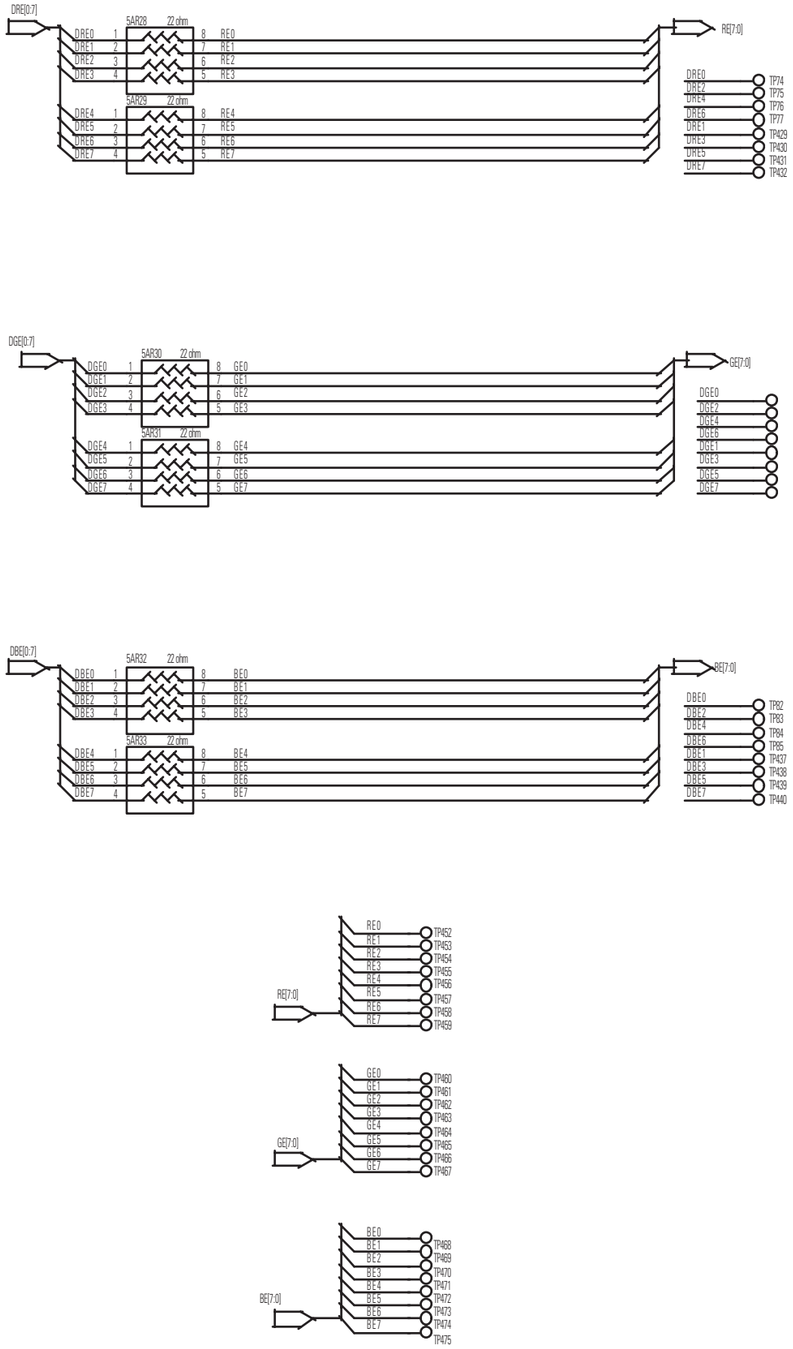
10-1-4 CONPONENT2 SIGNAL PROCESS



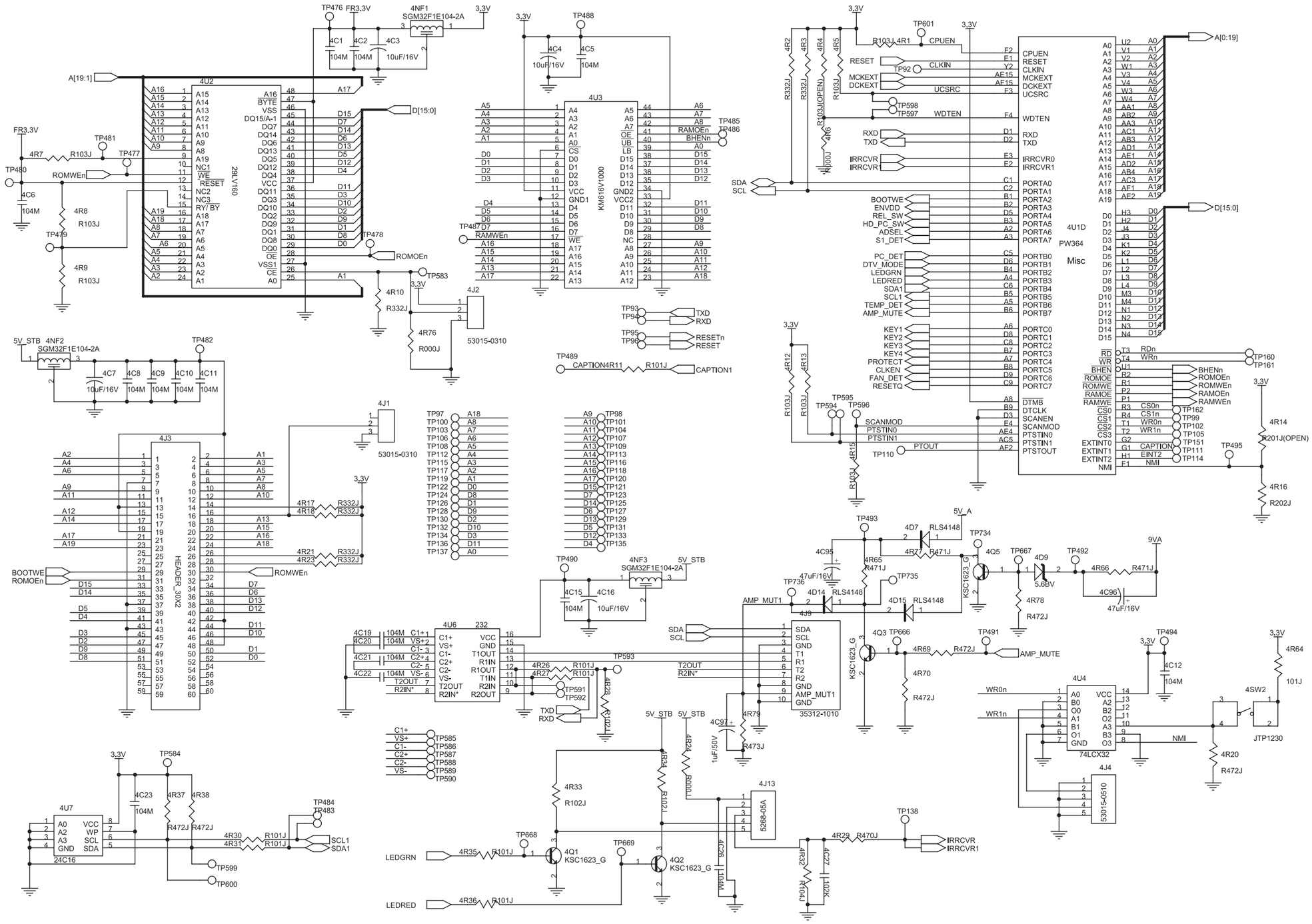
10-1-5 RGB INTERFACE



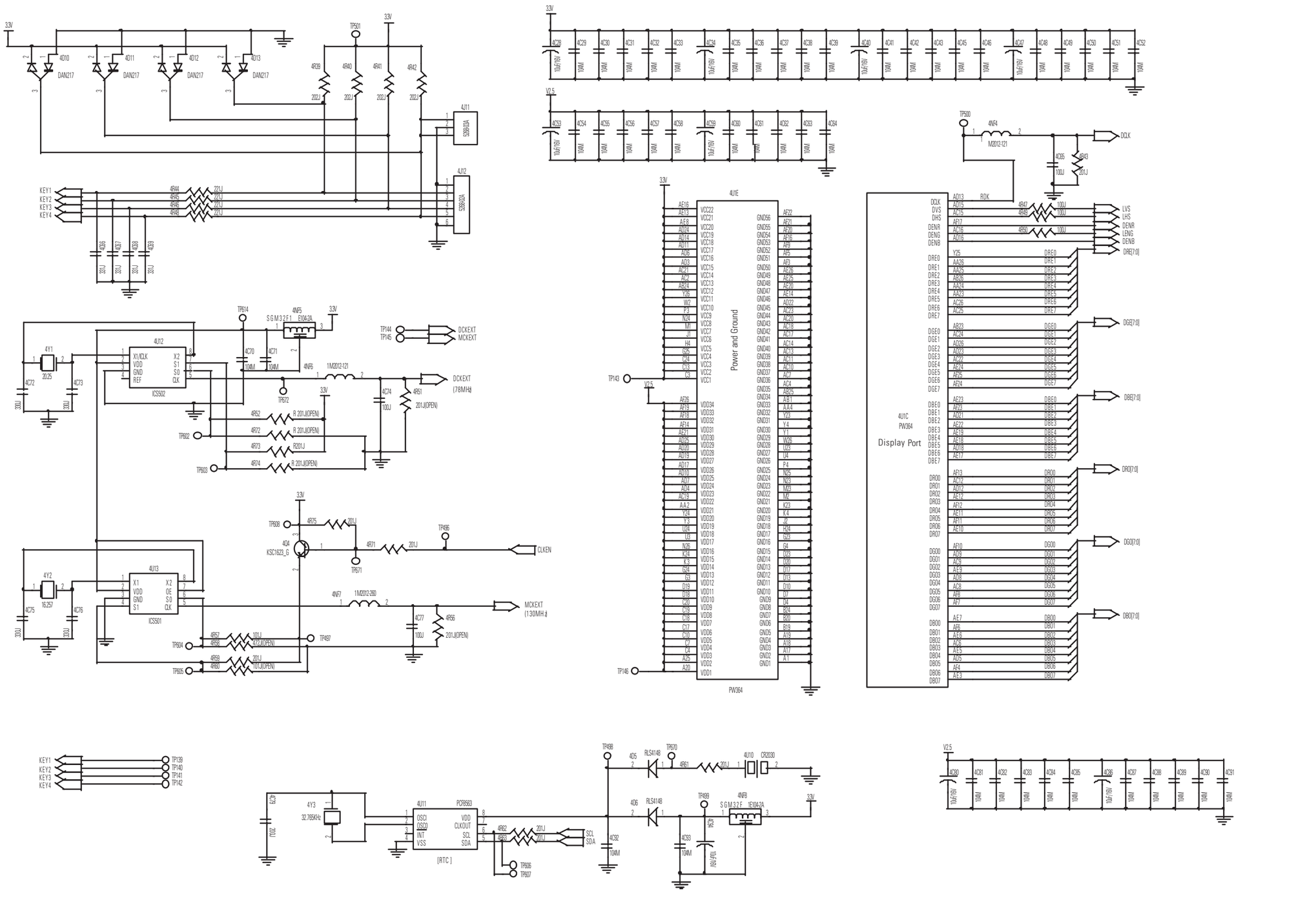
10-1-6 LVDS INTERFACE



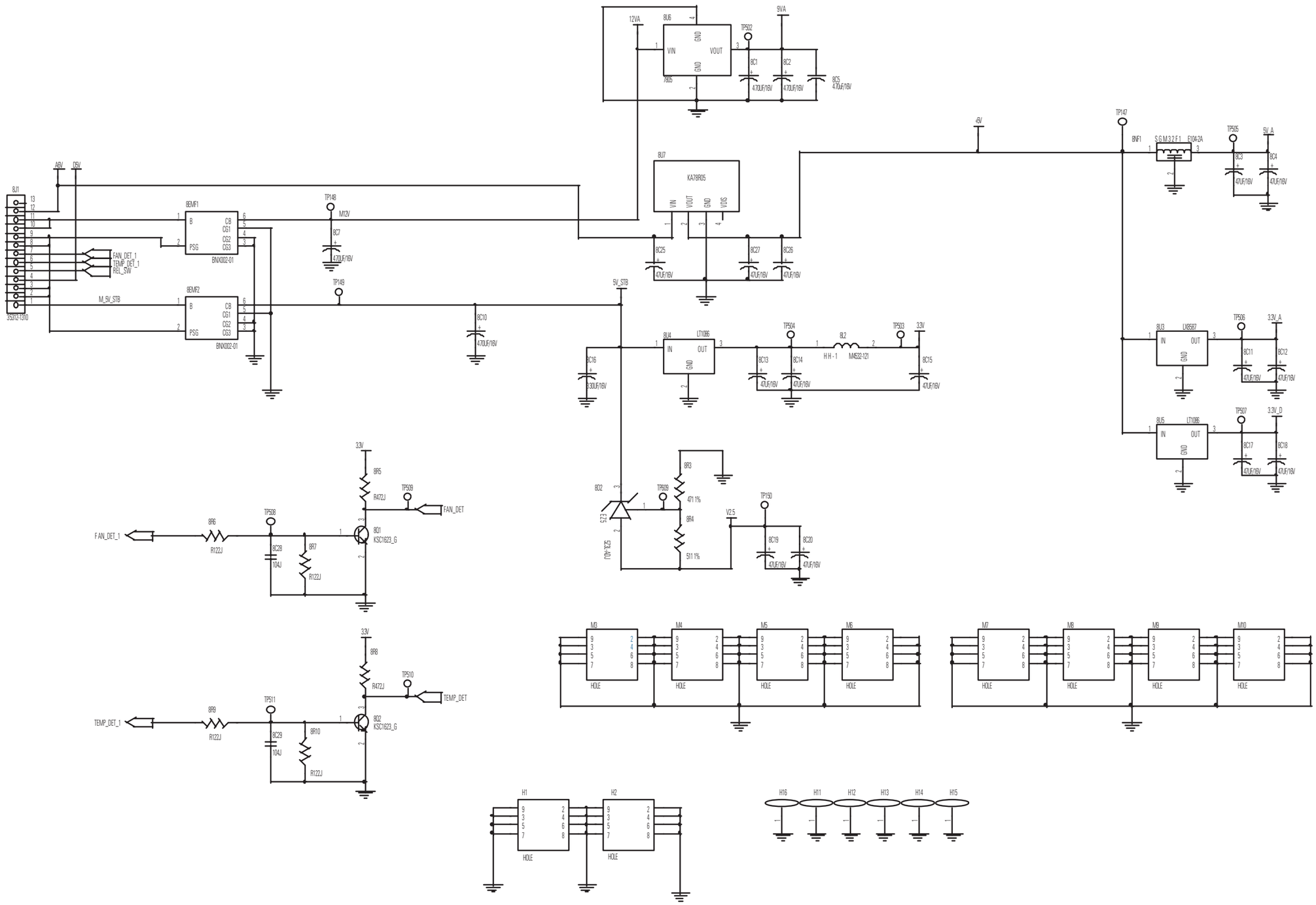
10-1-7 MEMORY INTERFACE & CONTROL INTERFACE`



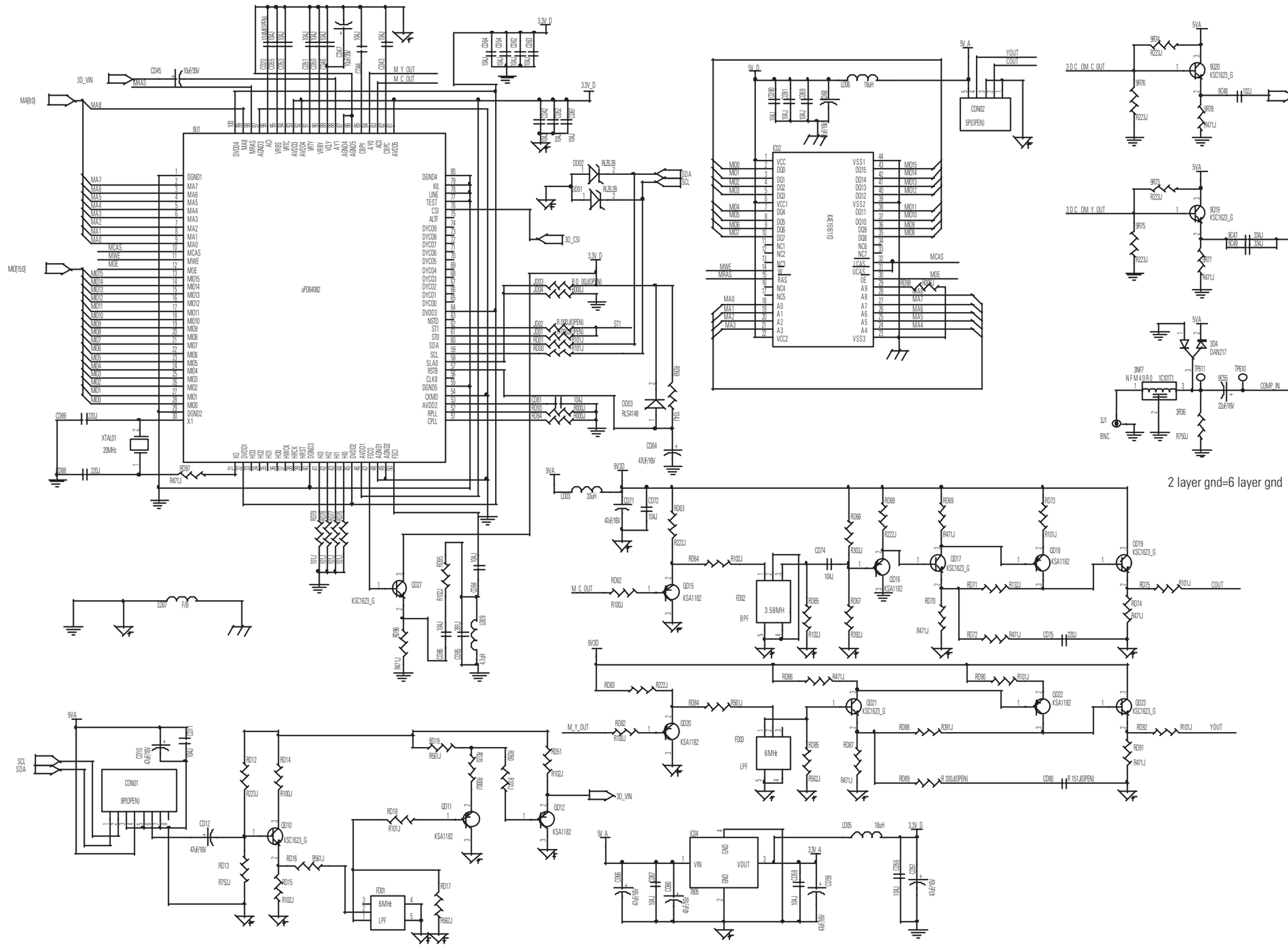
10-1-8 OUTPUT & PLLS OF SCALER



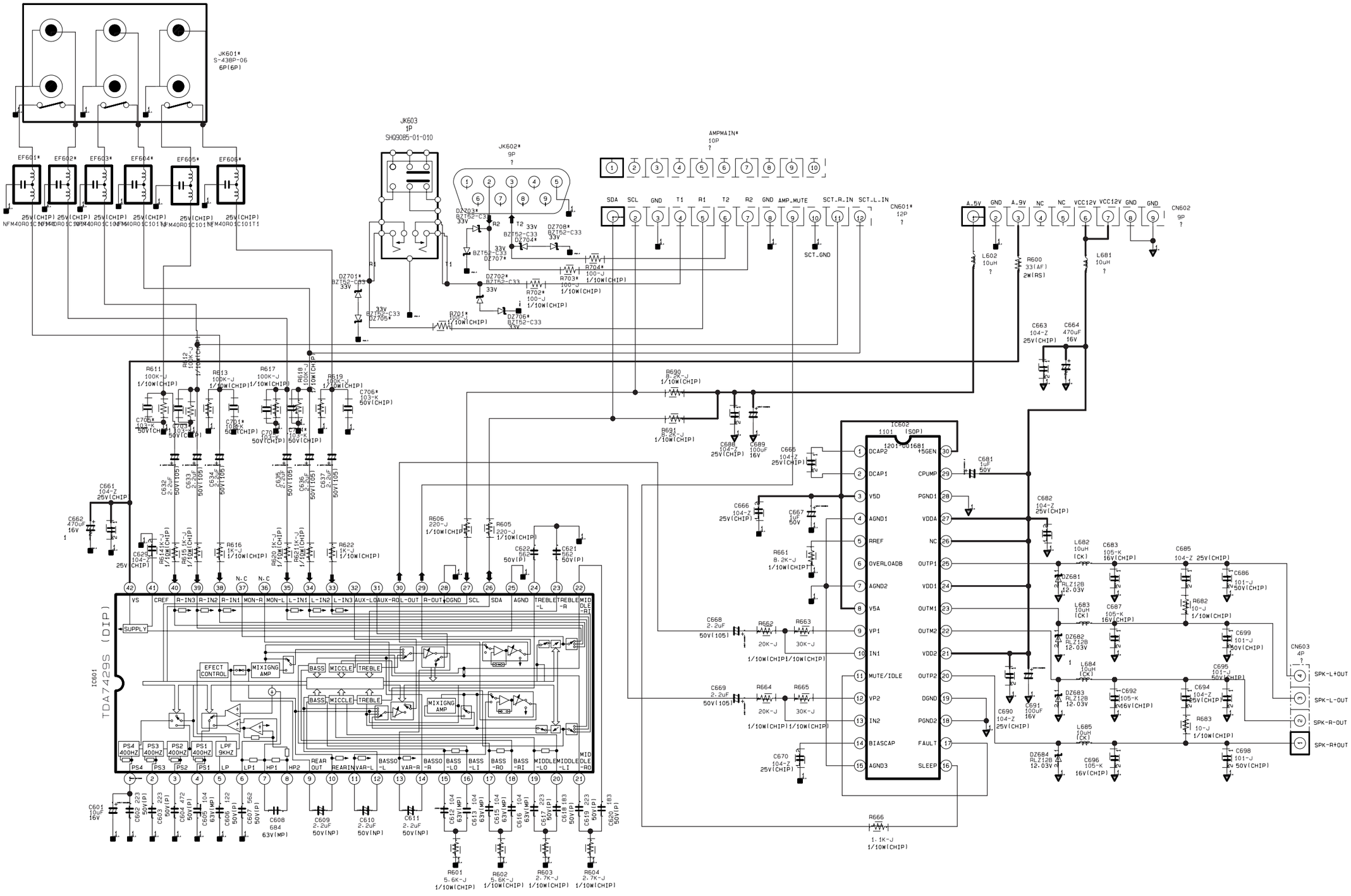
10-1-9 POWER


12VA
BU6
VIN
VOUT
GND
7805
TP502
5VA
BC1
BC2
BC5
470UF/16V
+5V
TP147
BNF1
S.G.M.3.2.F.1 F104-2A
TP505
5V_A
BC3
BC4
BU7
KA78R05
VIN
VOUT
GND
VOS
BC25
BC27
BC26
A5V
D5V
BJ1
35312-1310
BMF1
BNX002-01
FAN_DET_1
TEMP_DET_1
REL_SW
M_5V_STB
BMF2
TP148
M12V
BC7
TP149
5V_STB
BC10
BC16
330UF/16V
BU4
LT1086
TP504
BL2
HH-1 M4532-121
TP503
3.3V
BC13
BC14
BC15
BU3
LX8587
TP506
3.3V_A
BC11
BC12
BU5
TP507
3.3V_D
BC17
BC18
3.3V
BR5
R472J
TP509
FAN_DET
FAN_DET_1
TP508
BR6
R122J
BC28
104J
BR7
R122J
BD1
KSC1623_G
BR8
TP510
TEMP_DET
TEMP_DET_1
TP511
BR9
BC29
BR10
BD2
KSC1623_G
BD3
TP508
TP150
V2.5
BC19
BC20
BR3
471 1%
BR4
511 1%
M3
M4
M5
M6
M7
M8
M9
M10
HOLE
H1
H2
H16
H11
H12
H13
H14
H15

10-1-10 3D-COM

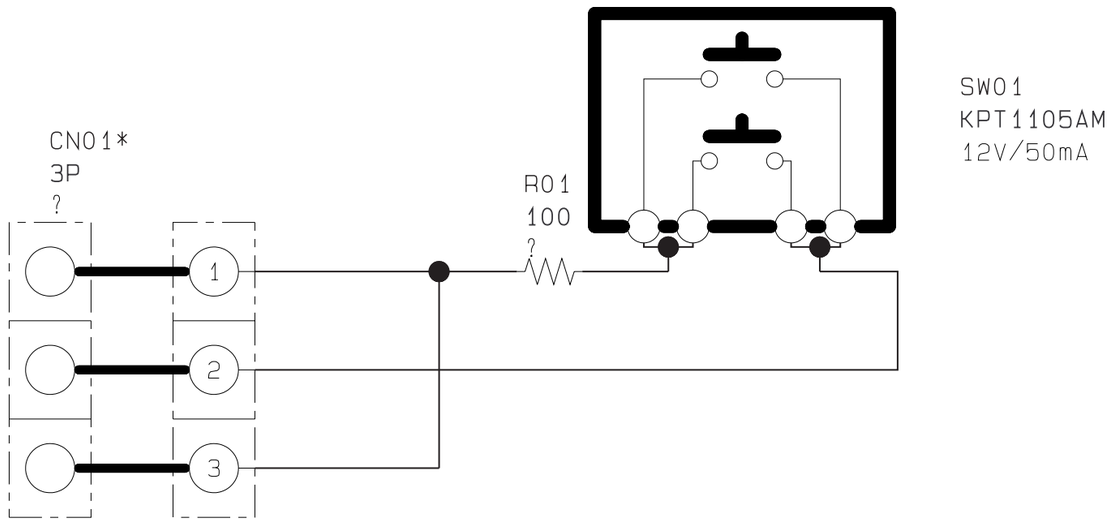

3D_VIN
MRAS
M_Y_OUT
M_C_OUT
3.3V_D
9U1
uPD64082
3D_CSI
SDA
SCL
XTAL01
20MHz
9V_D
9V_A
YOUT
COUT
IC02
MC15161D
MCAS
MWE
MOE
MRAS
5VA
3.D.C_OM C_OUT
3.D.C_OM Y_OUT
C1_OUT
Y1_OUT
COMP_IN
9V3D
9VA
QD19
KSC1623_G
QD21
QD22
QD23
QD15
KSA1182
QD16
QD17
QD18
QD20
QD10
QD11
QD12
QD27
3.58MH
BPF
6MHz
LPF
CON01
8P(OPEN)
CON02
5P(OPEN)
IC04
7805
3.3V_A
18uH
33uH
2 layer gnd=6 layer gnd

10-2 SOUND

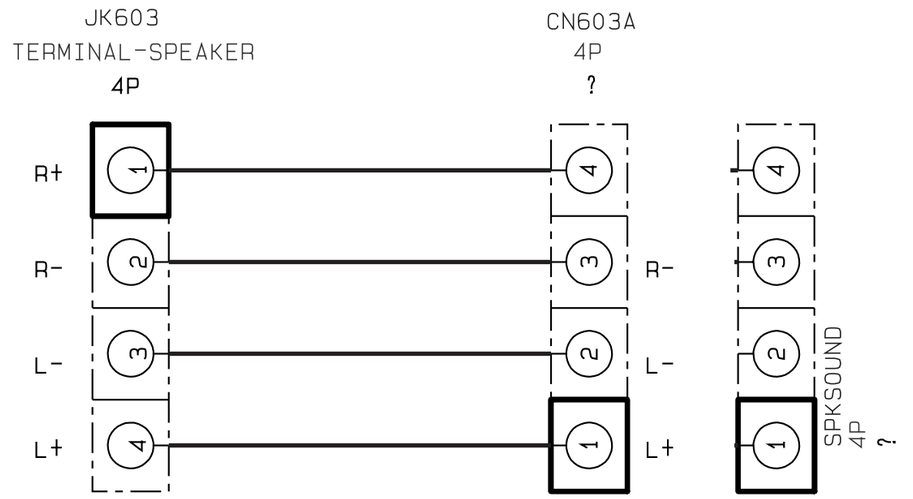

JK601*
S-438P-06
6P(6P)
EF601*
EF602*
EF603*
EF604*
EF605*
EF606*
JK603
1P
SH09085-01-010
JK602*
9P
AMPMAIN*
10P
SDA
SCL
GND
T1
R1
T2
R2
GND
AMP_MUTE
SCT_R_IN
SCT_L_IN
CN601*
12P
SCT_GND
A_5V
GND
A_9V
NC
NC
VCC12V
VCC12V
GND
GND
CN602
9P
L602
10uH
R600
33(AF)
2W(RS)
L681
10uH
C663
104-Z
25V(CHIP)
C664
470uF
16V
IC601
TDA7429S (DIP)
SUPPLY
EFECT CONTROL
MIXIGNG AMP
BASS
MICCLE
TREBLE
PS4 400HZ
PS3 400HZ
PS2 400HZ
PS1 400HZ
LPF 9KHZ
IC602
1101 (SOP)
1201-001681
DCAP2
DCAP1
V5D
AGND1
RREF
OVERLOADB
AGND2
V5A
VP1
IN1
MUTE/IDLE
VP2
IN2
BIASCAP
AGND3
+5GEN
CPUMP
PGND1
VDDA
NC
OUTP1
VDD1
OUTM1
OUTM2
VDD2
OUTP2
DGND
PGND2
FAULT
SLEEP
SPK-L+OUT
SPK-L-OUT
SPK-R-OUT
SPK-R+OUT
CN603
4P

10-3 POWER SWITCH / SPK TERMINAL

POWER SWITCH



SPK TERMINAL



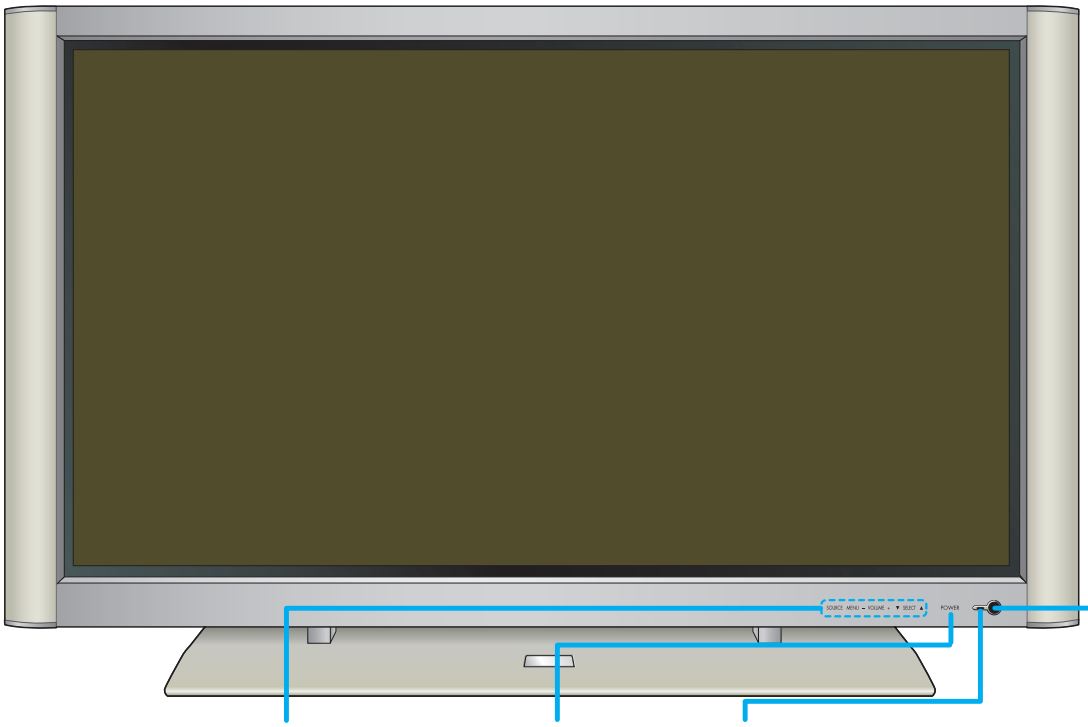
8. Handling Description

8-1 Basic Description

8-1-1 The Name of Each Part

8-1-1(A) PDP(Plasma Disply Panel)

Front Panel



SOURCE, MENU, VOLUME (-,+), SELECT (t,s), MUTE

POWER

Press to turn the PDP on and off.

POWER Indicator

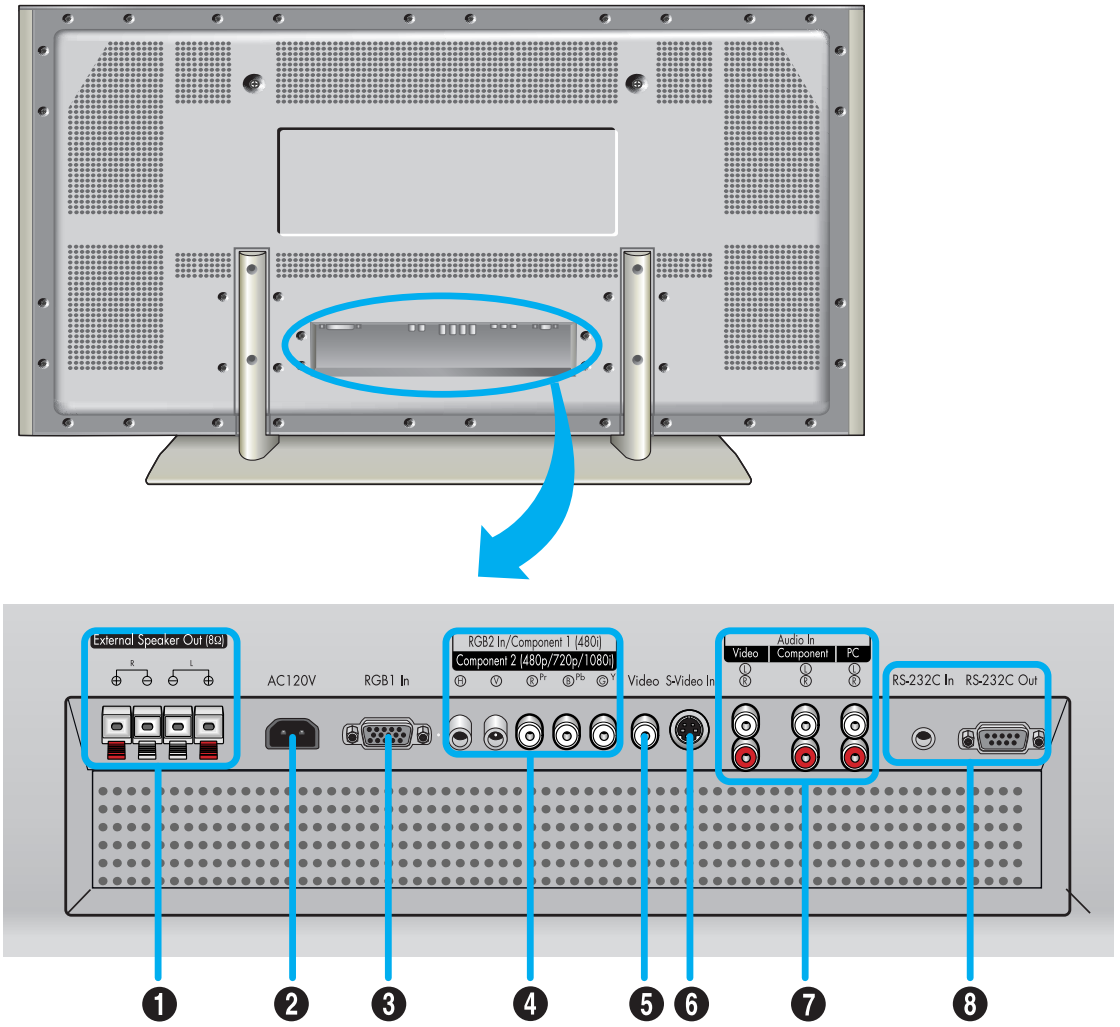
When TV set is on, this indicator will be lighted Green.

When TV set is off, this indicator will be lighted Red.

Remote Control Signal Receiver

Aim the remote control towards this spot on the Monitor.

Real Panel



❶ External Speaker Out jacks

Connect external speakers.

❷ Power Input jack

Connect the included power cord.

❸ RGB Input 1 jack (15pin)

Connect to the video output jack on your PC.

❹ RGB Input 2 / Component Video Input jacks (H / V / R / G / B, Y / Pb / Pr)

RGB input2 / Component video input jacks are BNC connectors.

❺ Video Input jack

Connect a video signal from external sources like VCRs or DVD players.

(Video / Component / PC) jacks

❻ S-VHS Input jack

Connect a S-Video signal from an S-VHS VCRs or DVD players.

❼ Audio Input (Video / Component / PC) jacks

Connect a audio signal from external sources like VCRs, PC or DVD players.

❽ RS-232C Input / Output jacks

Only for service. Power Input jack

Connect the included power cord.

8-1-1(B) REMOTE CONTROL BUTTONS

Remote Control

Filp the cover open in the arrow direction.

❶ Power button
Turns the PDP on and off.

❷ Number buttons

❸ Display button
Press to display information on the PDP screen.

❹ Menu button
Displays the main on-screen menu.

❺ CH (Channel) and VOL (Volume) buttons
Channel and Volume buttons are used for selecting menu item in menu mode.

❻ Mute button
Press to mute the PDP sound.

❼ P.Mode button
Adjust the PDP picture by selecting on of the preset factory settings (or select your personal, customized picture settings.)

❽ Aspect button
Press to change the screen size.

❾ Mode button
Selects a target device to be controlled by the samsung remote control (ie., VCR, Cable, or DVD players).

❿ Clock Display button
Press to display clock on the PDP screen.

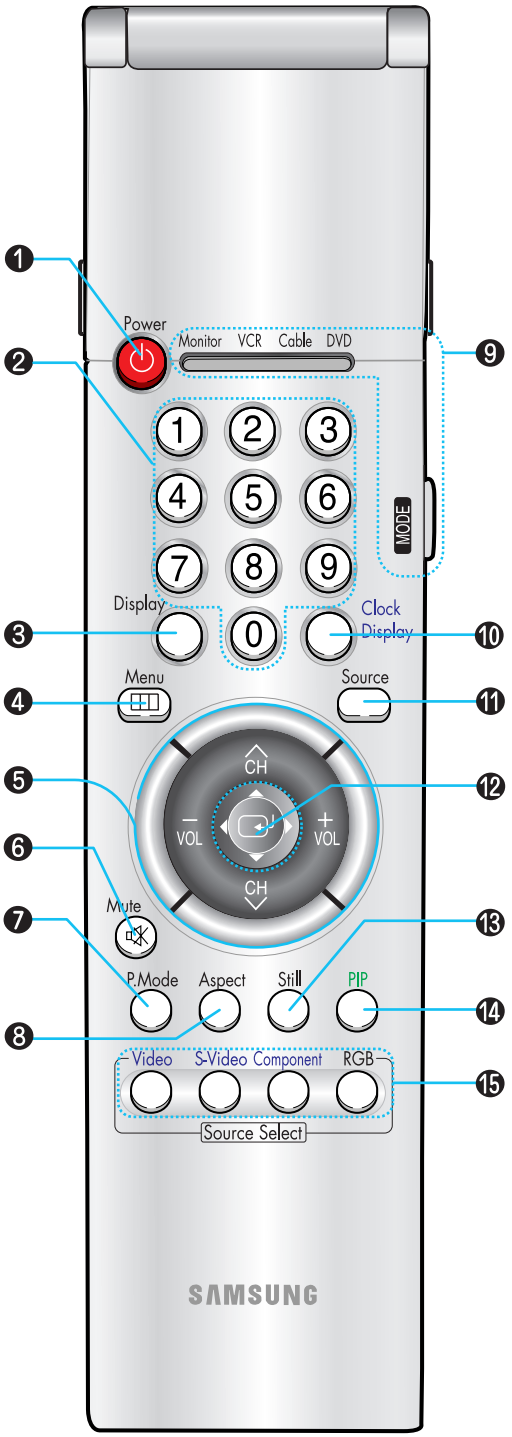
⓫ Source button
Press to display all of the available video sources (ie., Video, S-Video, Component1, Component2, PC).

⓬ Joystick button
Use to highlight on-screen menu items and change menu values.

⓭ Still button
Press to pause the current screen.

⓮ PIP button
Activates picture in picture.

⓯ Source selection buttons
Press to directly select Video, S-Video, Component1, Component2 or PC.



⑯ VCR control buttons
Controls VCR tape functions: Stop, Rewind, Play / Pause, Fast Forward.

⑰ Set button
Use during setting up of this remote control, so that it will work compatibly with other devices (VCR, cable box, DVD, etc.)

⑱ Clock set button
Press to clock setting.

⑲ PIP control buttons
Source : Press to select one of the available signal sources for the PIP window.
S.Sel : Press to select the Audio (PIP or Main).
Locate : Press to move the PIP window to any of the screen.

⑳ PC control buttons
Auto Adjust
Scaling
Zoom / Pan

㉑ S.Mode button
Adjust the PDP sound by selecting one of the preset factory settings (or select your personal, customized sound settings.)

㉒ Sleep button
Press to select a preset time interval for automatic shutoff.

8-2 Wall Mount

8-2-1 Notice for installing

1 Do not install the PDP on any place other than vertical walls.

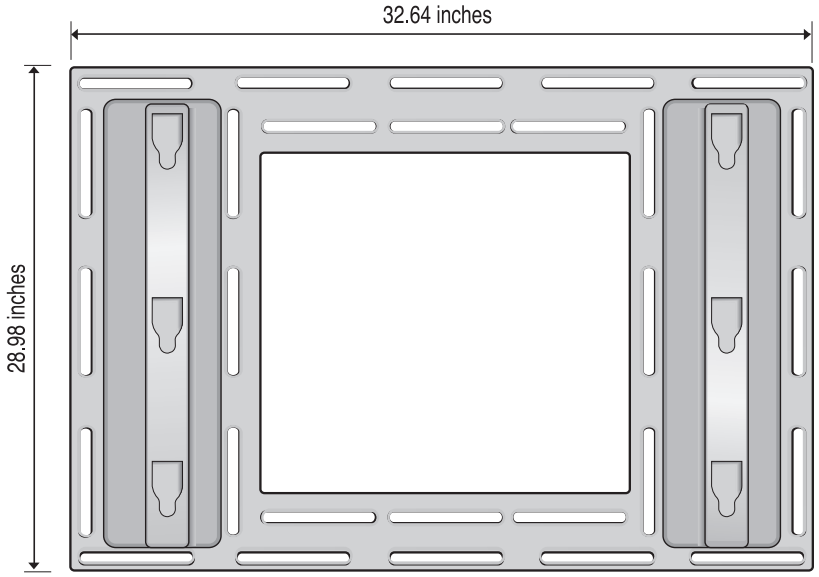
2 To protect the performance of the PDP and prevent troubles, avoid the following.

- Do not install next to smoke and fire detectors.
- Do not install in an area subjected to vibration.
- Do not install in an area subjected to high voltage.
- Do not install near or around any heating apparatus.

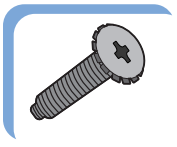
3 Use only recommended parts and components.

4 Do not install in the wall.

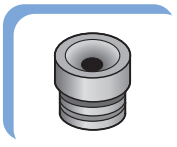
8-2-2 Parts(wall attachment panel is sold separately.)



Wall attachment panel(mm)



bolt

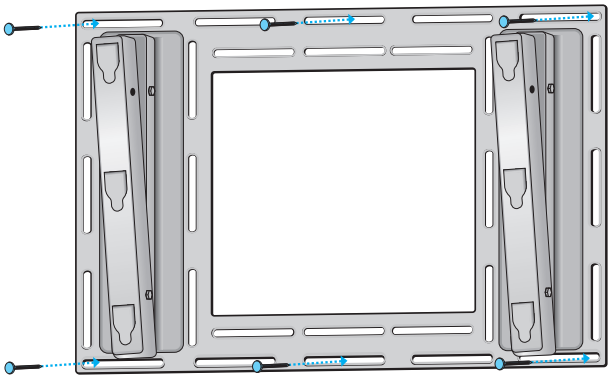


Insulation rubber

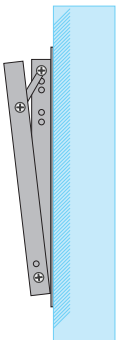
8-2-3 Installing the Display on the Wall Attachment Panel :

1. See the drawing of the wall attachment panel shown in page 14 to check for the stability of the wall where the PDP is to be installed. If the wall is not enough strong to support the PDP, strengthen the wall before installation.

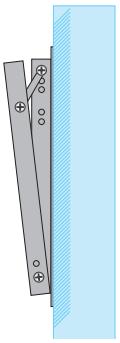
2. Fix the wall attachment panel on the wall using bolts as shown in the following figure: Fixing bolts must protrude from the wall appox. 0.6 inches.



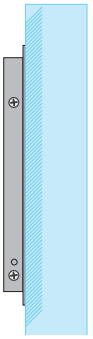
3. Using the wall attachment panel, you may adjust the angle of the display from 0 to 15 degrees. The angle can be set in 5 stages with 5 degrees of distance each using the angle control holes on the sides of the panel.



When the angle has been set to 5 degrees.

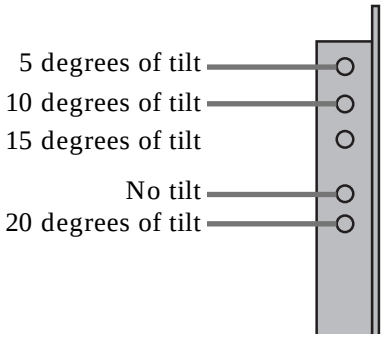


When the angle has been set to 15 degrees.

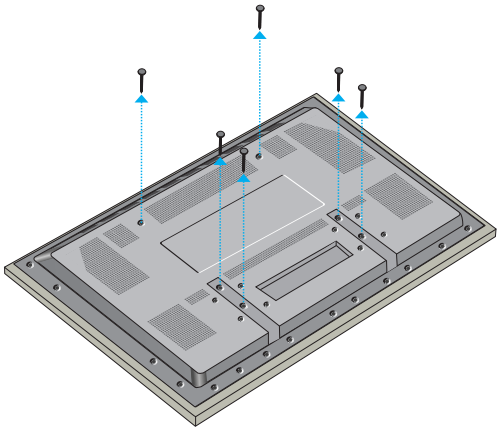


When the panel hasn't been tilted.

Angle control holes



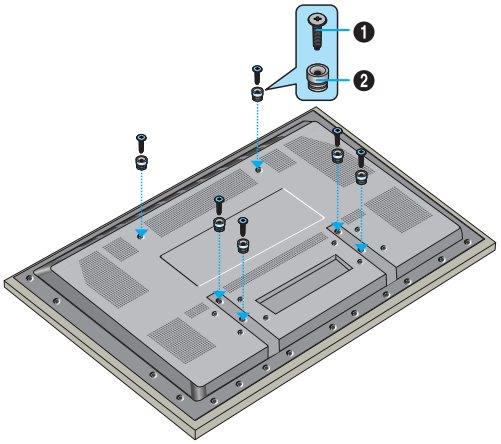
4. Remove six large screws from the rear side of the display.



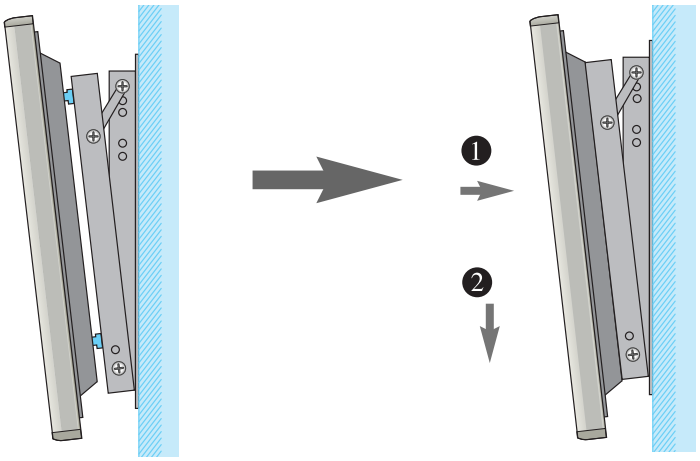
5. Insert the bolts, dish-type washers,
and insulation holder into the six screwholes as shown in the following figure:

❶ Bolt

❷ Insulation rubber

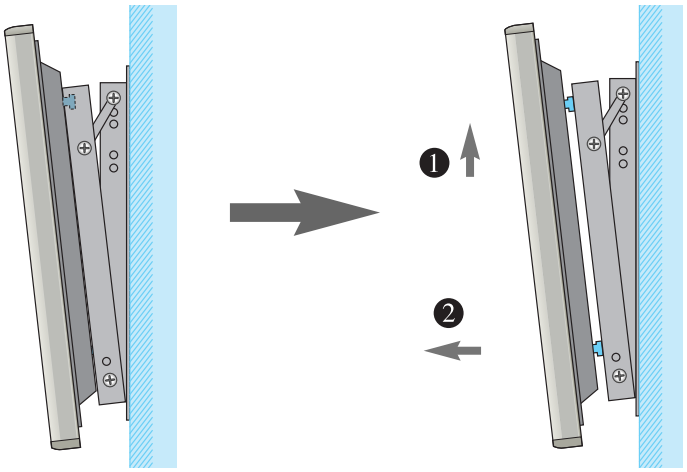


6. Hang the protruding plastic part on the rear of the PDP up the groove on the top of the wall attachment panel. Then, lift down the PDP. (Do not lift down the PDP with too much force. The protruding plastic part might be taken off.)



8-2-4 Separating the Display from the Wall Attachment Panel :

After lifting the PDP up, pull it forward and remove it from the wall attachment panel.



9. Glossary

AC PDP :
Plasma display driven by alternating current plasma electric discharge.

Address discharge(Reference : scan and data) :
Term with two meanings that can be used for both scan and data (write or erase) discharge.

Address Electrode(Reference : scan and data electrode) :
Term with two meanings that can be used for both scan and data electrodes.

Address pulse(Reference : scan and data pulse) :
Address drive wave form

Address voltage(reference; scan and data voltage) :
Address drive amplitude of vibration

Addressing :
Process that gives authorization to cells to allow for turning on and off by drive wave form.

Addressing speed :
Time necessary for writing and erasing.

ADS, address display separation :
Drive tech that separates address pulse temporarily from sustained voltage.

Aging :
The change of operation expectancy- for example, operation voltage change and luminance decline-related characteristics.

Angular distribution :
Characteristics which change as function of angles between perpendicularity and surface.
referring to dependency on angles of, for example, luminance or chromaticity.

Aperture ratio :
Referring to the ratio of an element activation area to the gross area.

Area luminance :
Luminance measured in relatively large area.

Aspect ratio :
The ratio of screen width to height.

Auto power control :
Circuit means for controlling panel's average or maximum power.
Auxillary anode :
Anode where discharge of DC panel has little contribution to light output power.

Back ground luminance :
Referring to the panel luminance in off mode or black screen, in other words, luminance in the vicinity of the screen.

Barrier rib :
barriers that cross all the gaps of wafers dividing the cells in panel.

Black stripe :
black substance located in between the fluorescent areas to bring about improvement in contrast by reflection ratio decline. Generally, this is striped.

Bright defect :
defects that occur when the image is rather bright than accurate.

Brightness(Reference : luminance) :
visible and subjective quality, for example, how bright matters look or how much visible rays are perceived.
Notice) Do not get confused luminance with brightness because those two are not the same. Brightness is subjective while luminance is objective.

Brun in :
element's initial operation section that takes place until the element stabilizes or the initial expectancy expiration is detected.

Bus electrode :
aggregate of sustained electrodes that are bussed together.

Cathode electrode :
cathode electrified electrode that releases electrode from element. In AC plasma panel, polarity switches in every half a cycle.

Cell :
capacity corresponding to each electric discharge. In general, it is defined by the shape of substrates and electrodes but can be defined by partitions.

Cell gap :
measurements identifying the gaps between substrates.

Cell pitch :
measurement that identifies the cells from the surface of substrates. It varies depending on the direction of rows and columns.

Charge transfer curves :
curves expressing the quantity of electric charge that is transferred, as the function of drive wave form characteristics.(for example, voltage, time and others)

Color arrangement(in other words, sub-pixel arrangement) :
term expressing the location of one pixel consisted of sub color pixels.

Color coordinates, CIE 1931 :
Color image expressing method in color dimension, originated from CIE standard of 1931, expressed by X, Y and Z. Among those three, Y element corresponds to luminous flux that is expressed as lumen while X and Y are values that express red and purple element of luminous flux. Colors of matter are expressed as color coordinates pair (x, y). Here $x=X/(X+Y+Z)$, $y=Y/(X+Y+Z)$.
Method for colors, known as (u, v), where image colors are expressed in more even color dimension. Colors of matter are expressed as color coordinates pair (u, v). Here, $u=4X/(X+15Y+3Z)$, $y=6Y/(X+15Y+3Z)$.

Color coordinates, CIE 1960 :
Method for colors, known as (u, v), where image colors are expressed in more even color dimension. colors of matter are expressed as color coordinates pair(u, v). Here, u=4X(X+15Y+32), y=6Y / (X+15Y+32Z).

Color coordinates, CIE 1976
Method for colors, known as (u', v'), where revised image colors are expressed in more even color dimension. v' is 1.5-fold of recommended v value of 1960. The color of matter is expressed as color coordinates pair (u', v'). Here, u'=4X / (X+15Y+3Z) , v'= 9Y / (X+15Y+3Z).

Color coordinates, CIE 1976 CIELUV and CIELAB :
Three dimensional parameters expressing with u' and v' including Ω√∞®º∫ against chromaticity and luminance of standard white light in display. Among the parameters, only CIELUV gets to have proper color space where additional two blend light appears in line segment. (refer to CIE Publication 15.2, Colorimetry 1st edition 1976, 2nd edition 1986)

Color depth :
The number of digital bit alocated to each major color.

Color gamut :
Physically realizable color space area.

Color reproducibility (Refer to color gamut) :
The expression of realizable colors limited by color information distinction or fluorescent substance chromaticity.

Color temperature, correlated (symbol CCT) :
Seemingly temperature expressed with absolute temperature of black body radiation with the closest chromaticity. This can be expressed as CCT, in the form of C. S. McCamy. CCT=437N3+3601n2+5517, n=(x-0.3320) / (0.1858-y) and x, y=color coordinates of CIE 1931.

Columm electrode :
Vertically successive electrodes. It generally refers to data electrodes. When panel is installed along the photograph, this can be arranged along the horizontal direction.

Concurrent driving method :
Driving method to disperse address pulse and scan pulse at equal distance.

Contrast ratio Columm electrode :
Ratio of white luminance to black luminance of image. This measurement has many parameters, so measurers are required to explain the consideration for measurement to make understood the meaning of the measurement. The parameters of contrast ratio are as follows.

- CA - ratio of center luminance in all white screen to center luminance of all black screen on the condition of light being spreading around.
- CG - ratio of white luminance to black luminance in successive arrangement of white and black lines at equal distance.
- CL - ratio of white luminance to black luminance in white line against black screen of black line against white screen.
- CR - the ratio of white luminance to black luminance.

- Cm - Michelson contrast or contrast modulation:
  Here, Lw is the luminance of the color white while Lb is the luminance of the color black.

- CT - Threshold contrast ratio: the minimum contrast ratio that is permissive, in general.

Chip on board(COB) :
PCB with IC on substrate.

Dark defect :
Defects in the brighter image realization than normal one.

Data electrode :
Electrodes allowed for controlling electric discharge by changing the cell's state to switch on from off (and vise versa) in AC plasma panel.

Data electrode driver :
Driving circuit to be attached to dada electrode.

Data write pulse :
Wave form for data electrode that switches from off to on.

Data erase pulse :
Wave form for data electrode that switches from on to off.

DC PDP :
Display panel whose plasma discharge is driven by direct current.

Decay time :
Time required for parameters to drop from certain level to another. It can be time necessary for dropping from 90% to 10%, or to e-1 level of the initial value, or to certain irreversibility.

Dielectric layer :
Dielectric layer with larger sustained electric constant.

Discharge :
1. neutralization of electric charge (for example, voltage decrease of capacitor)
2. electric current flow in dielectric media such as gas.

Discharge current :
Discharge electric current.

Discharge electrode :
Another term for sustained electrode.

Discharge efficiency :
Another term for gloss efficiency

Discharge gap :
The gap among sustained electrodes in discharge space of three-electrode plasma panel.

Discharge slit :
(Refer to discharge gap)

Displacement current :
Electric current flow through capacitor that includes atomic rearrangement of discharge within electric matter.

Display color number (color number possible to be displayed with other words.) :
displayable individual color's number.

Display Diagonal :
Diagonal size of display contour

Display efficiency :
The ratio of gloss output divided by the entire display power.

Display height :
Height of display contour

Display scan electrode :
(Refer to scan electrode)

Display width :
Width of display contour

Displayed color :
Refer to displayed color number.

Displayed color number :
Color numbers that can be made by display.

Dot (Refer to cell, pixel and subpixel) :
The term is hard to be defined because it is not clear if the term refers to full color pixel or subpixel. The term is used when referring to color related elements that make up full color pixel or subpixel.

Dot pitch :
(Ambiguous expression. Refer to dot, cell pitch, pixel pitch and subpixel pitch.)

Driving waveform :
Expressing ∞ÊΩ√ change of driving signal voltage.

Driving scheme :
Expressing the thought applying driving voltage to display.

Effcacy :
Refer to luminous efficacy.

Energy recovery circuit :
Circuit degauss caught after reusing the power that drove AC plasma panel.

Erase :
Process where cells are erased from AC plasma panel.

Erase pulse :
Cell erasing waveform

Erase voltage :
Erase pulse voltage required for erasing cells from AC plasma panel.[symbol : Ve]

Evacuating (Interchangeable terms : evacuation, exhaust) :
Process where unwanted gas is rid from device.

Exhaust tubulation (Interchangeable terms: exhaust tube, exhaust pipe) :
Tube shaped hole in device connected to external vacuum pump, for controlling the initiation from device during process. This is usually glass tube that prevents with flannelet after filling proper gas

Filling gas (Refer to gas mixture) :
After removing air, plasma panel goes through filling with proper electric and optical gas. Therefore, panel gas composition is commonly called "filling gas".

Firing voltage :
Minimum voltage where triggers discharge in plasma device[symbol : Vf]

Flicker :
Fast and instant changes in luminance, perceivable in almost regular luminance experiment pattern.

Front substrate :
Substrates closer to the viewers, made of transparent material such as glass

Full color display :
Full color image (for example, image with more than 8 bit color tone) realizable display

Fpc(Flexible Printed Curcuit) :
Flexible substrates with circuited copper foil on polyimide

Gas mixing ratio (Interchangeable terms: gas mixture, gas composition) :
Gas composition within plasma device. It is usually expressed with ratio of the constituent gas.

Gas voltage (Interchangeable terms: gas break down voltage) :
Voltage where electrode and ion within plasma device can generate additional electrodes and ions.
-Thus, increasing the electric current within the device sharply. (break down or overflowing)

Glass substrate :
Substrates consisted of glass

Glow discharge :
Plasma discharge taking place under pressure of tens of millimeter. This is defined by ionization generated by activated electrons in discharge space and electron release in cathode by ion bombardment.

Gradation :
Gradual change in characteristics such as luminance and chromaticity

Gray scale :
The range of luminance acquired when displayed from black to white.

High strain point glass :
Glass of which strain point (temperature with viscosity of 1014.5 poise) is relatively high

Image retention :
Continuous existence of image after the stimulation is removed.

Image sticking :
(Refer to Image retention.)

Interconnect pad groups :
A group of connection terminals that attach to individual connector. (also referred to as terminal block.)

Interconnect pad pitch :
Mutual measurements for individual of interconnect pad group.

Interconnect pad spacing :
The size of non-electric conductive area between individual terminal.

Inter-electrode gap :
In Three electrodes plasma panel, the measurement of sustained voltage separated from outside discharge space.

Ion bombardment :
The bombardment of energetic ions in the surface of solid matter. The transfer of kinetic energy toward surface from ions can cause electron release, ion or neutron release and temperature change in surface.

Life time :
Time during device exerts its function. Commonly known as mean time failure (MTTF).

Low melting point glass :
Glass of which melting point (temperature with viscosity of 1014.5 poise) is relatively low.
Since glass is non- crystalline, the word melting is not appropriate, but it gets more fluid as it becomes hot.

Luminance :
Colloquial term for measurement of brightness of display.
It also refers to display related CIE Y constituent. it is expressed by cd / m2.

Luminance efficacy :
It refers to gloss output against the total display consumption power. It is calculated by the value generated through dividing gloss output of ∞Ì^{a}Û white substance with gross consumption power. It is expressed as lumen / watt.

Luminance efficiency :
Gloss output value according to consumption power increase, calculated by the value generated through dividing gloss output of ∞Ì^{a}Û white substance with white screen power consumption increase against black screen. It is expressed as lumen / watt.

Luminance loading :
Luminance decline that takes place when white square luminance increases into full size all white square.

Matrix(type) PDP :
Plasma display panel made up of matrix with rows and columns.

Matrix type :
Refer to matrix PDP
Maximum firing voltage :
Voltage value required for triggering discharge in all cells.

Maximum sustain voltage :
Maximum drive voltage required not to turn off the cells.

Memory margin :
The disparity between the maximum sustained voltage for keeping discharge and the sustained voltage for turning off the cells

Memory type PDP :
Refer to AC Plasma Panel that has memory. PDP made up of cells that keep turned on or off until switch occurs.

MgO layer :
In bombardment of electrons and ions, MgO's high electron release rate, like cathode application, makes it easier to release electrons.

MgO protecting layer (Refer MgO layer) :
MgO layer on fluorescent material has secondary benefit that prevents fluorescent degradation by ion bombardment.

Minimum firing voltage :
Minimum voltage that can turn on any cells.[symbol : V1]

Minimum sustain voltage :
Minimum sustain voltage that keeps turned on cell on.[symbol : Vsm1]

Monochrome display Minimum sustain voltage :
Display that only expresses a limited color such as white, green and amber.

Multi-color display :
Display that can express multiple colors .if not all colors.

Non-discharge slit :
(Refer to inter electrode gap)

Operating margin :
AC PDP voltage range that keeps cells turned on or off. Generally, its value gets less than memory margin because of additional factors such as temperature effect, gloss ionization effect and waveform change.

Operating window :
Actual voltage range that keeps cells turned on or off in any drive levels and surrounding environment.

Operating window degradation :
Gradual decline in operating window, according to operating time.

Opposed discharge :
Traditional two-electrode plasma panel structure where discharge occurs between the two sustained electrodes across from each other.

Opposed discharge PDP :
(Refer to opposed discharge.)

Peak luminance :
Maximum luminance generated in one pixel in panel.

Peak luminance enhancement :
Circuit and drive technology that accommodates increasing peak luminance.

Phosphor degradation :
Gradual decline in fluorescence efficiency according to operating expectancy.

Phosphor layer :
Thin layer made up of phosphor. Fluorescenc**Pl**e substance must be thick enough to optimize transferring the ultraviolet rays from plasma discharge to visible light

Pixel, picture element :
The smallest unit that can display the entire range of luminance and chromaticity. Generally, pixel consists of sub pixels (or dots).

Pixel arrangement :
Expression of sub pixels within a pixel.

Pixel count :
The number of pixels that make up a display. It is described as the number of column pixels against the number of row pixels.

Pixel pitch :
The distance between the centers of the two closest pixels. Move as far as the pitch and reach the identical location.

Plasma display :
Electrically driven display device for causing electric discharge in gas within device. Electric energy generates light with atomic light release or from proper colored fluorescence substance.

Positive column discharge :
The plasma area for long glow discharge. This area is a low electric field but relatively electric conductive plasma area.

Pre discharge :
Cell's state where pre discharge is taking place. In this case, cell's state becomes electric conductive due to formation of discharge generated by ionization process of gas.

Priming :
The stage where ions are generated for forming discharge. Generally, this is required for injection.

Priming pulse :
Electric waveform to define the proper conditions for the next cell discharge.[symbol : Pp]

Priming voltage :
Voltage of priming pulse.[symbol : Vp]

Protecting layer :
The layers applied to the device function constituents (for example, fluorescence, electrode and glass layers).

Quantum efficiency :
Substrates farther from the viewers. These can be opaque.

Rear substrate :
Efficiency measurement that is directly expressed with the number of output particles against the number of input particles. In case of plasma panel, the number of photons in visible area, generated from photons in ultraviolet area

Reset :
(Refer to erase.)

Reset discharge, Reset pulse :
(Refer to erase.)

Resolution :
Display's ability to enable to distinguish the matters close to each other. It is confusing with addressibility that generates pattern undistinguishable to the eyes.

Row electrodes :
Horizontally successive electrodes. In terms of traditional drive concept, these are the sustained electrodes. If the panel is installed toward portrait, these row electrodes can be arranged horizontally.

Sand discharge :
Process where grinding of surface occurs. It is used for making three dimensional surface in lithography or silt in sheet.

Scan discharge :
Discharge injected along the pair of sustained electrodes.

Scan electrode :
Electrodes of the pair of sustained electrodes that inject discharge downward along the panel columns.

Scan pulse :
Waveform that injects discharge with new columns.
Optic defects where scratches display over certain size.

Seal :
Combining the substrates or substrate with ventilation tube.

Seal layer :
Material layer that provides the connection of substrates. This can be a single layer of solder glass (frit) or the combination of solder glass and ring.

Sealing :
Process where free electrons that get out of the surface by extracting static electricity field when energetic electrons or ions are limited to a surface.

Secondary electron emission :
Process where drags discharged cell to certain waveform. This could occur before ionization offset when cell voltage decreases.

Self erase :
Plasma display in the form where stimulating discharge occurs for discharge process precedes below panel.

Self-scan type PDP :
Plasma display in the form where stimulating discharge occurs for discharge process precedes below panel.

Self-shift type PDP :
Process of combining substrates. High temperature process that melts solder glass combining substrates.

Space charge :
Mutual repulsion caused by accumulation of electric charge of similar signal.

Stripe rib :
Stripe shaped partition structure. It follows panel column direction.

Sub frame :
(Refer to sub field)

Sub field :
A part of panel

Surface charge :
It refers to the location of discharge in AS plasma panel where sustained electrodes are on the same surface.

Surface charge PDP :
AS plasma panel where sustained electrodes are on the same surface.

Sustain :
Discharge in AC plasma panel that keeps on or off until the cell is erased or written. Sustained electrodes are divided into bus (common electrodes) and addressable electrodes.

Sustain driver :
Circuit that drives sustained electrodes.

Sustain electrode :
Electrodes driven by AC voltage that provides plasma with energy major parts. This electrode is driven by enough waveform to keep discharge of turned on state. In turned off cell, trigger discharge does not takes place.

Sustain magin :
The disparity between sustained voltage that keeps turned on cells and sustained voltage that can turn off cells.

Sustain pulse :
Sustained drive waveform[symbol : Ps]

Sustain vlotage :
Voltage level of sustained waveform
Thermal compaction :
Substrates successive density increase observed by substrates pattern contraction.

Thermal radiation :
Radiation in infrared rays over 800nm.

Three electrode type :
Modern AC panel has three electrodes for each cell and a pair of thermal electrodes provide cells with AC power. Data electrodes in opposite substrates provide unique writing and erasing signals to each cell

Time modulation driving method (Other terms: time division multiplex method) :
Modulation method in proportion to certain time applied to stimulation with regular output. Output strength is changed according to input time.

Tip pipe :
(Refer to exhaust turbulation.)

Townsend discharge :
Self sustained plasma discharge expressed by Townsend in 1901. This discharge requires 200v voltage.

Transparent electrode :
Electrode made up of transparent electric conductive matter such as ITO.

Two eledtrode type :
Original AC plasma panel used two electrodes that provide not only sustained waveform but also write and erase waveform.

Ultraviolet ray :
Ultraviolet light below 380nm in spectrum.

Vacuum ultraviolet :
Ultraviolet ray of wavelength below 200nm.

Viewing angle :
Vertical angle that can display the image. It is normally limited by the change in luminance and chromaticity.

Viewrable screen diagonal :
Releasable screen diagonal length measured between outmost pixel edges

Viewrabel screen height :
Releasable screen height measured between outmost pixel edges

Viewrable screen width :
Releasable screen width measured between outmost pixel edges.

Visible defect :
Imperfection that prevents displaying with proper image.

Wall charge :
Pure accumulation of positive and negative charges in cell wall.

Wall charge erase pulse :
Pulse that neutralizes wall charge

Wall charge transfer curve :
Curve related to wall charge pulse parameters and the changes in wall charge.

Wall voltage transfer curve :
Curve expressed with wall transfer that is caused by any changes in electric charges including wall charges and wall charge pulse related parameters.

White back :
White coating for minimize absorbing valid gloss, located black contrast improvement layer and fluorescent material.

Write electrode :
(Refer to data electrode.)

Write electrode :
(Refer to data electrode)[symbol : Pw]

Write electrode :
(Refer to data electrode)[symbol : Vw]

M E M O